IEEE PROPOSED MICROCOMPUTER SYSTEM BUS STANDARD — P796 BUS

PROPOSED
MICROCOMPUTER SYSTEM BUS STANDARD
(P796 BUS)

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Bibliography

Intel Multibus™ Specification

1. General

1.1 Scope. One of the most important elements in a computer system is the bus structure that supplies the interface for all the hardware components. This bus structure contains the necessary signals to allow the various system components to interact with each other. It allows memory and I/O data transfers, direct memory accesses, generation of interrupts, etc. This document provides a detailed description of all the elements and features that make up the 796 Bus.

The bus supports two independent address spaces: memory and I/O. During memory cycles, the bus allows direct addressability of up to 16 megabytes using 24-bit addressing. During I/O bus cycles, the bus allows addressing of up to 64K I/O ports using 16-bit addressing. Both memory and I/O cycles can support 8-bit or 16-bit data transfers.

The bus structure is built upon the master-slave concept where the master device in the system takes control of the bus and the slave device, upon decoding its address, acts upon the command provided by the master. This handshake (master-slave relationship) between the master and slave devices allows modules of different speeds to be interfaced via the bus. It also allows data rates up to five million transfers per second (bytes or words) to take place across the bus.

Another important feature of the bus is the ability to connect multiple master modules for multiprocessing configurations. The bus provides control signals for connecting multiple masters in either a serial or parallel priority fashion. With either of these two arrangements, more than one master may share bus resources.

This document has been prepared for those users who intend to evaluate or design products that will be compatible with the 796 system bus structure. To this end, the necessary signal definitions and timing and electrical specifications have been covered in detail.

This standard deals only with the interface characteristics of microcomputer devices: not with design specifications, performance requirements, and safety requirements of modules.

Throughout this standard, the term "system" denotes the byte or word interface system that, in general, includes all the circuits, connectors, and control protocol to effect unambiguous data transfer between devices. The term "device" or "module" denotes any product connected to the interface system that communicates information via the bus, and that conforms to the interface system definition.

1.2 Object. This standard is intended:

(1) To define a general purpose microcomputer system bus.

(2) To specify the device-independent electrical and functional interface requirements that a module shall meet in order to interconnect and communicate unambiguously via the system.

(3) To specify the terminology and definitions related to the system.

(4) To enable the interconnection of independently manufactured devices into a single functional system.

(5) To permit products with a wide range of capabilities to be interconnected to the system simultaneously.

(6) To define a system with a minimum of restrictions on the performance characteristics of devices connected to the system.

1.3 Definitions. The following general definitions apply throughout this standard. More detailed definitions can be found in the appropriate section.

1.3.1 *General System Terms*

Compatibility. The degree to which devices may be interconnected and used without modification, when designed as defined in Sections 2 and 3 of this standard. Section 5 introduces the notion of levels of compliance and the corresponding notation.

Bus cycle. The process whereby digital signals effect the transfer of data bytes or words across the interface by means of an interlocked sequence of control signals. "Interlocked" denotes a fixed sequence of events in which one event must occur before the next event can occur.

Interface. A shared boundary between two systems, or between parts of systems, through which information is conveyed.

Interface system. The device-dependent electrical and functional interface elements necessary for communication between devices. Typical elements are: driver and receiver circuits, signal line descriptions, timing and control conventions, and functional logic circuits.

Override. A bus master overrides the bus control logic when it is necessary to guarantee itself back-to-back bus cycles. This is called "overriding" or "locking" the bus, temporarily preventing other masters from using the bus.

System. A set of interconnected elements which achieve a given objective through the performance of a specified function.

1.3.2 *Signals and paths*

Bus. A signal line or a set of lines used by an interface system to connect a number of devices, and to transfer information.

Byte. A group of eight adjacent bits operated on as a unit.

Word. Two bytes or sixteen bits operated on as a unit.

High state. The more positive voltage level used to represent one of two logical binary states.

Low state. The more negative voltage level used to represent one of two logical binary states.

Signal. The physical representation of data.

Signal level. The relative magnitude of a signal when compared to an arbitrary reference. Signal levels in this standard are specified in volts.

Signal line. One of a set of signal conductors in an interface system used to transfer messages among interconnected devices.

Signal parameter. That element of an electrical quantity whose values or sequence of values convey information.

2. Functional Description

This section provides an overall understanding of how the 796 Bus functions, and describes the elements that connect to the bus, the signals that provide the interface to the bus, and the different types of operations performed on the bus.

In this section, as well as throughout the specification, a clear and consistent notation for signals has been used. The Memory Write Command (MWTC) will be used to explain this notation. The terms one:zero and true:false can be ambiguous, so their use will be avoided. In their place, we will use the terms electrical High and Low (H and L). A nathan (asterisk) following the signal name (MWTC*) indicates that the signal is active low as shown:

MWTC* = Asserted at 0 volts

The signal (MWTC*) driven by a three state driver will be pulled up to V_{CC} when not asserted. The following is used to further explain the notation used in this specification.

Function	Definition Electrical	Definition Logic	State
MWTC	H	1 True	Active, Asserted
	L	0 False	
MWTC*	L	1 True	Active, Asserted
	H	0 False	

2-1. 796 Bus Elements. This subsection describes the elements (masters and slaves) that interface to the bus and the 796 bus signal lines that comprise this interface.

2.1.1 *Masters.* A master is any module having the ability to control the bus. The master exercises this control by acquiring the bus through bus exchange logic and then generating command signals, address signals, and memory or I/O addresses. To perform these tasks, the master is equipped with either a central processing unit or logic dedicated to transferring data over to the bus to and from other destinations. Fig. 1 depicts a system that includes a master and two slave models.

The 796 Bus architecture can support more than one master in the same system, but in order to do this, there must be a means for each master to gain control of the bus. This is accomplished through the bus exchange logic (see 2.4).

Masters may operate in one of two modes of operation. Modes 1 and 2 are defined as follows:

Mode 1: Masters are limited to single bus transfers per bus connect. If all masters are Mode 1, system timing is rendered deterministic by conformance with a maximum bus busy period. That period is limited by the paramter t_{BYSO} max. (see 3.2.5).

Mode 2: Masters are unlimited in ths bus control. They may invoke bus override. Bus timeouts are allowed. Conformance with the maximum busy period is not required.

The last classification is included to allow for a very broad class of operations, giving users maximum flexibility in meeting these applications' needs. The first mode of operation is defined to allow system designers to predict the overall performance of their systems without concern for uncontrolled timing parameters such as bus timeout. For Masters which can only operate in Mode 2, their specification shall state "Mode 2 master only."

2.1.2 *Slaves.* Another type of module that can interface to the bus is the slave. Slave modules decode the address lines and act upon the command signals from the masters. The slaves are not capable of controlling the bus. Some examples of bus slaves are shown in Fig. 1.

2.1.3 *796 Bus Signals.* Signals transferred over the bus can be grouped into several classes based on the functions they perform. The classes are:

(1) Control Lines

(2) Address and Inhibit Lines

(3) Data Lines

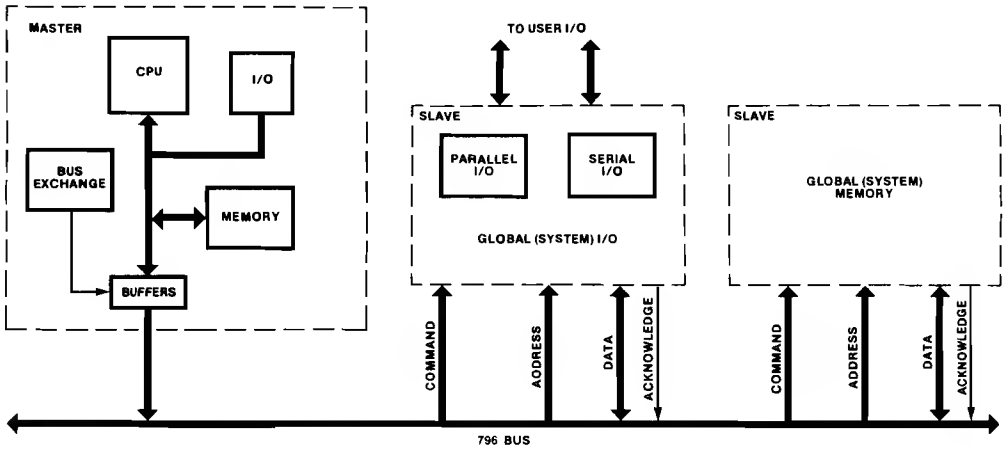


Fig. 1
796 Bus Master and Slave Example

(4) Interrupt Lines

(5) Bus Exchange Lines

The following subsections explain the different classes of 796 Bus signals.

2.1.3.1 *Control Lines.* The following signals are classified as control lines:

Class	Function	Signal
Clocks	Constant Clock	CCLK*
	Bus Clock	BCLK*
Commands	Memory Write	MWTC*
	Memory Read	MRDC*
	I/O Write	IOWC*
	I/O Read	IORC*
Acknowledge	Transfer Acknowledge	XACK*
Initialize		INIT*
Lock		LOCK*

2.1.3.1.1 *Clock Lines.*

(1) *Bus Clock (BCLK*).* A periodic signal used to synchronize the bus contention logic; it may be slowed, stopped, or single stepped. The Bus Clock shall be generated by one and only one source within the system. This means that each standalone bus master must have the capability of generating an acceptable clock that can optionally be connected to, or disconnected from, the bus. In a multimaster system, only one of the masters shall have its clock connected to the bus.

(2) *Constant Clock (CCLK*).* A periodic signal of constant frequency, which may be used by masters or slaves as a master clock. The Constant Clock shall be generated by one and only one source within the system. This means that each bus master must have the capability of generating an acceptable clock that can optionally be connected to, or disconnected from, the bus. In a multimaster system, only one of the masters shall have its clock connected to the bus.

2.1.3.1.2 *Command Lines (MWTC*, MRDC*, IOWC*, IORC*).* The command lines are elements of a communication link between the masters and slaves. There are two command lines for memory and two command lines for I/O. An

active command line indicates to the slave that the address lines are carrying a valid address, and that the slave is to perform the specified operation. In a data write cycle, the active command line (MWTC* or IOWC*) additionally indicates that the data is valid on the bus. In a data read cycle, the transition of the command (MRDC* or IORC*) from active to inactive indicates that the master has received the data from the slave.

2.1.3.1.3 *Transfer Acknowledge Line (XACK*).* This line is used by the slaves to acknowledge commands from the master. XACK* indicates to the master that the requested action is complete, and that data has been placed on, or accepted from, the data lines.

2.1.3.1.4 *Initialize (INIT*).* The INIT* signal is generated to reset the entire system to a known internal state. This signal is usually generated prior to starting any operations on the system. INIT* may be generated by any or all of the bus masters or by an external source such as a buffered and debounced front panel switch.

2.1.3.1.5 *Lock (LOCK*).* The LOCK signal is generated by the master in control of the bus to indicate the bus is locked. LOCK* is used to extend mutual exclusion to multiple port ram designs.

2.1.3.2 *Address and Inhibit Lines.* The address and inhibit lines are used for the following signals:

Function	**Signal**
Address Lines	ADR0*-ADR17* (0-9, A-F, 10-17 in hexadecimal)
Byte High Enable	BHEN*
Inhibit Lines	INH1* and INH2*

2.1.3.2.1 *Address Lines (24 lines).* These lines, which specify the address of the referenced memory location or I/O device, allow a maximum of 16 megabytes (16,777,216 bytes) of memory to be accessed. When addressing an I/O device, a maximum of 16 address lines (ADR0*-ADRF*) are used, thus allowing the

addressing of a maximum of 64K devices. An I/O module must also be able to be configured to decode only 8 address lines (ADR0*-ADR7*) and ignore the upper 8 lines (see 2.2.2.3).

2.1.3.2.2 *Byte High Enable Line (BHEN*).* This byte control line is used to enable the upper byte (bits 8-F) of a 16-word bit word to drive the bus. The signal is used only on systems that incorporate 16-bit memory modules.

2.1.3.2.3 *Inhibit Lines (INH1* and INH2*).* The inhibit lines can be invoked for any memory read or memory write operation (MRDC* or MWTC*). An inhibit line is asserted by a slave to inhibit another slave's bus activity during a memory read or write operation. The inhibit signal generated by the inhibiting slave is derived from decoding the memory address lines. The inhibiting slave can decode a single address, a block of addresses, or any combination of single and block addresses.

When it detects the specific address during an actual command (MRDC* or MWTC*), the inhibiting slave generates an inhibit signal, which is sensed by the inhibited slave. When so inhibited, this slave module disables its drivers from all data, address, and acknowledge bus lines, although it may actually perform internal operations. (All modules that may be inhibited must have completed internal operations within 1.5 microseconds from the start of the command line. This interval [1.5 microseconds] is also the minimum acknowledge timing for modules issuing inhibits. This guarantees that inhibited modules have enough time to return to their normal state before the current bus command is completed.)

2.1.3.3 *Data Lines (DAT0*-DATF*).* These 16 bidirectional data lines transmit and receive information to and from a memory location or an I/O port. (DATF* is the most-significant bit and DAT0* is the least-significant bit). In 8-bit systems, only lines DAT0*-DAT7* are valid.

2.1.3.4 *Interrupt Lines.* The interrupt lines consist of the following signals:

Function	Signal
Interrupt Requests	INT0*-INT7*
Interrupt Acknowledge	INTA*

2.1.3.4.1 *Interrupt Request Lines (INT0*-INT7*).* Interrupts are requested by activating one of the eight interrupt request lines. INT0* has the highest priority and INT7* has the lowest priority.

2.1.3.4.2 *Interrupt Acknowledge (INTA*).* In response to an Interrupt Request signal, an Interrupt Acknowledge signal can be generated by a bus master with bus vectored interrupt capability. The Interrupt Acknowledge signal is used to freeze the interrupt status and request the placement of the interrupt vector address on the bus data lines.

2.1.3.5 *Bus Exchange Lines.* The bus exchange lines are used by the following signals:

Function	Signal
Bus Clock	BCLK*
Bus Request	BREQ*
Bus Priority	BPRN*, BPRO*
Bus Busy	BUSY*
Common Bus Request	CBRQ*

A master gains control of the bus through the manipulation of these signals.

2.1.3.5.1 *Bus Request (BREQ*).* A signal used by the bus masters in a priority resolution circuit to indicate a request for control of the bus.

2.1.3.5.2 *Bus Priority (BPRN* and BPRO*).* The priority functions allow masters to break deadlocks that occur when more than one master concurrently requests the bus. The Bus Priority In (BPRN*) signal indicates to a particular master that no higher priority master is requesting use of the bus. The Bus Priority Out (BPRO*) signal is used in serial (daisy chain) bus priority resolution schemes. In such a scheme, BPRO* is passed by one master to the BPRN* input of the master with the next lower bus priority; when active, the BPRO* signal indicates that the higher priority master does not require control of the bus.

2.1.3.5.3 *Bus Busy (BUSY*).* A signal activated by the master in control of the bus to indicate that the bus is in use. This prevents other masters from gaining control of the bus.

2.1.3.5.4 *Common Bus Request (CBRQ*).* A signal that maximizes a master's data transfer rate to the bus by sensing the absence of other bus requests. The CBRQ* signal does this by serving two functions. It indicates to the master controlling the bus whether or not another master needs to gain control of the bus. To the other masters, it is a means of notifying the controlling bus master that it must relinquish control of the bus if it is not using the bus.

2.2 Data Transfer Operation. The primary function of the 796 Bus architecture is to provide a path for the transfer of data between modules on the bus. The following subsections describe the different types of data transfers and the means by which they are implemented using the signals previously described. Fig. 2 can be referenced during the following discussion.

The discussion of the data transfer operation of the bus is covered in three parts:

(1) An overview of the operation

(2) A detailed description of the signals used in the transfer

(3) A discussion of the specifics pertaining to the different transfers

It is assumed in this discussion that there is only one master on the bus, and therefore no bus contention exists. (The bus exchange logic is discussed in 2.4).

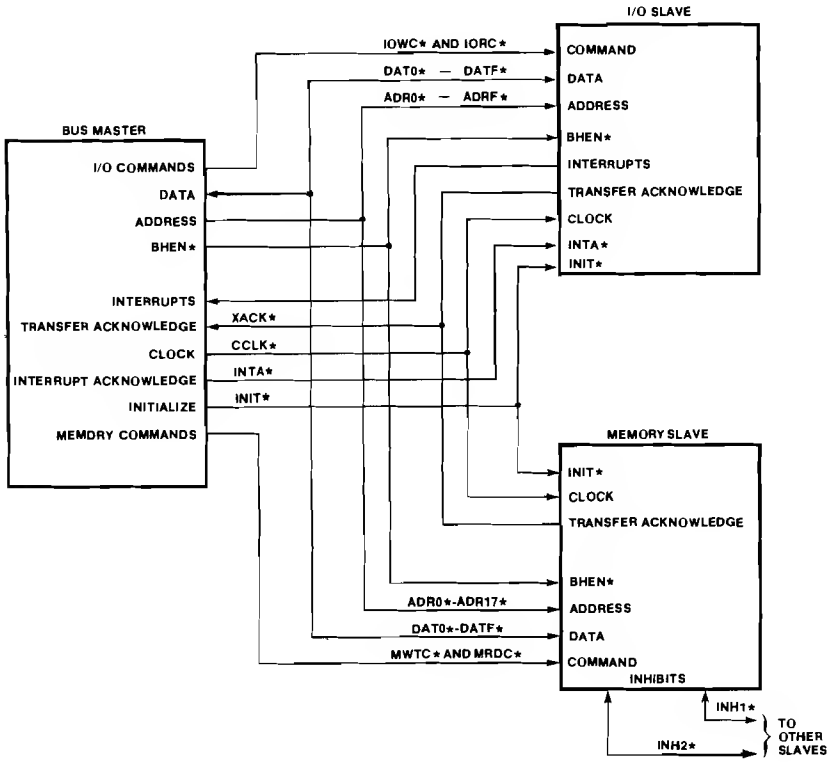


Fig. 2
796 Bus Interface Lines

2.2.1 *Data Transfer Overview.* A data transfer is accomplished as follows. First the bus master places the memory address or I/O port address on the address lines. (If the operation is a write, the data would also be placed on the data lines at this time.) The bus master then generates a command (I/O read or write, or memory read or write), which activates the appropriate bus slave. The slave accepts the data if it is a write operation, or places the data on the data lines if it is a read operation. A Transfer Acknowledge signal is then sent to the bus master by the bus slave, allowing the bus master to complete its cycle by removing the command from the command line and then clearing the address and data lines. Fig. 3 and Fig. 4 show the basic timing for a read and write data transfer operation.

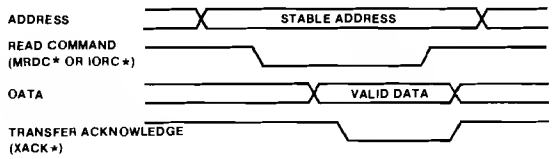


Fig. 3
796 Bus Read Operation

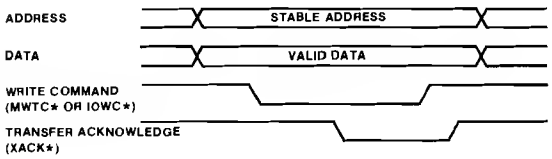


Fig. 4
796 Bus Write Operation

2.2.2 *Signal Descriptions.* This subsection provides a detailed description of the 796 Bus signals. Included are timing, signal origination, and other information pertaining to the specific function that each signal performs in the data transfer operation.

2.2.2.1 *Initialize (INIT*).* Prior to any operation of the bus, all system modules should be reset to a known internal state. This can be accomplished by an INIT* signal initiated by one of three sources:

(1) A power-on clear circuit (RC network), which holds INIT* low until the power supplies reach their specific voltage outputs

(2) A reset button, which is sometimes provided on the system front panel for operator use. Note that this button must be debounced

(3) A software command that can be implemented to pull down the INIT* line.

The INIT* line is driven by open-collector gates and requires signal conditioning to meet the electrical specifications of the bus.

2.2.2.2 *Constant Clock (CCLK*).* The Constant Clock signal, which is driven by only one source, provides a timing source for any or all modules on the bus. CCLK* is a periodic signal with a specified frequency and is driven by a clock driver circuit.

2.2.2.3 *Address Lines (ADR0*-ADR17*).* The address lines are used to specify the address of the memory location or the I/O device that is being referenced by the command. There are 24 address lines, binary coded, to allow up to 16,777,216 bytes of memory to be referenced. These lines are driven by three-state drivers and are always controlled by the master using the bus.

For I/O bus cycles, master modules have the option of generating 8 bit or 16 bit addresses. Because of this, all I/O slaves must be capable of being configured to decode 8 address bits (ADR0*-ADR7*) and ignore the upper address bits or to decode all 16 bits of address (ADR0*-ADRF*). Note that in a system using 8 bit I/O addresses, the value of the upper 16 bits of address is unknown. A master generating only 8 bit address may set the upper 16 address bits to any arbitrary value.

Refer to Fig. 5 for an example of address line usage.

2.2.2.4 *Data Lines (DAT0*-DATF*).* These are 16 bidirectional data lines used to transmit and receive information to and from a memory location or I/O port. The 16 lines are driven by the master on write operations and by the addressed slave (memory or I/O) on read operations. Both 16-bit and 8-bit transfers can be accomplished by using only lines DAT0*-DAT7* (with DAT0* being the least-significant bit).

There are three types of transfers that take place across the bus:

(1) Transfer of low (even) byte on DAT0*-DAT7*

(2) Transfer of high (odd) byte on DAT0*-DAT7* (using swap byte function)

(3) Transfer of a 16-bit word

Fig. 6 shows the data lines, and the contents of these lines for the three types of transfers mentioned.

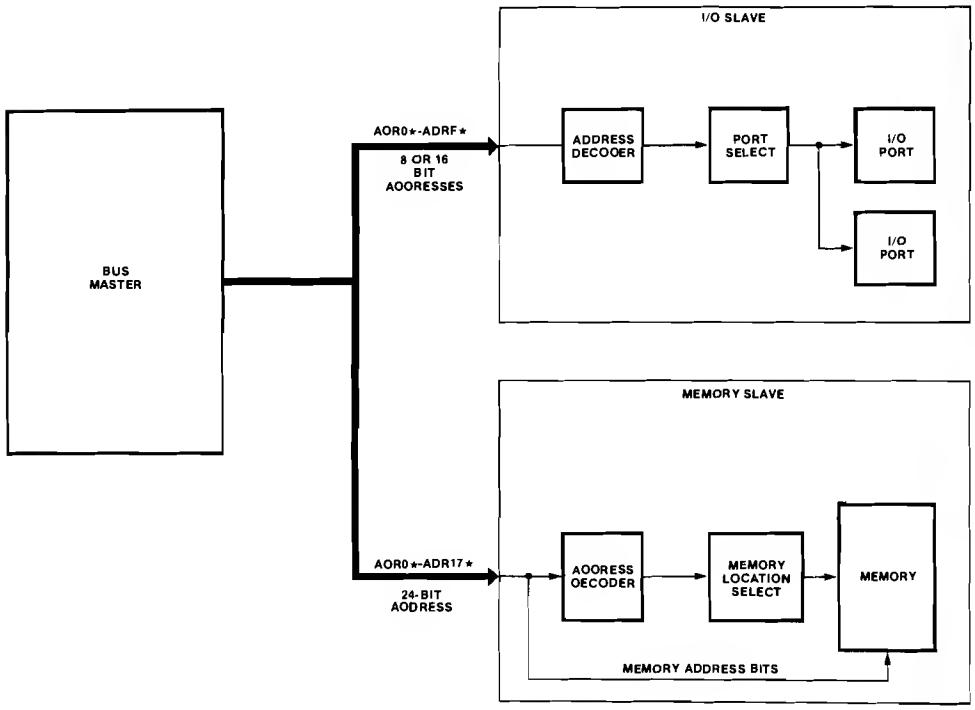


Fig. 5
796 Bus Address Line Usage

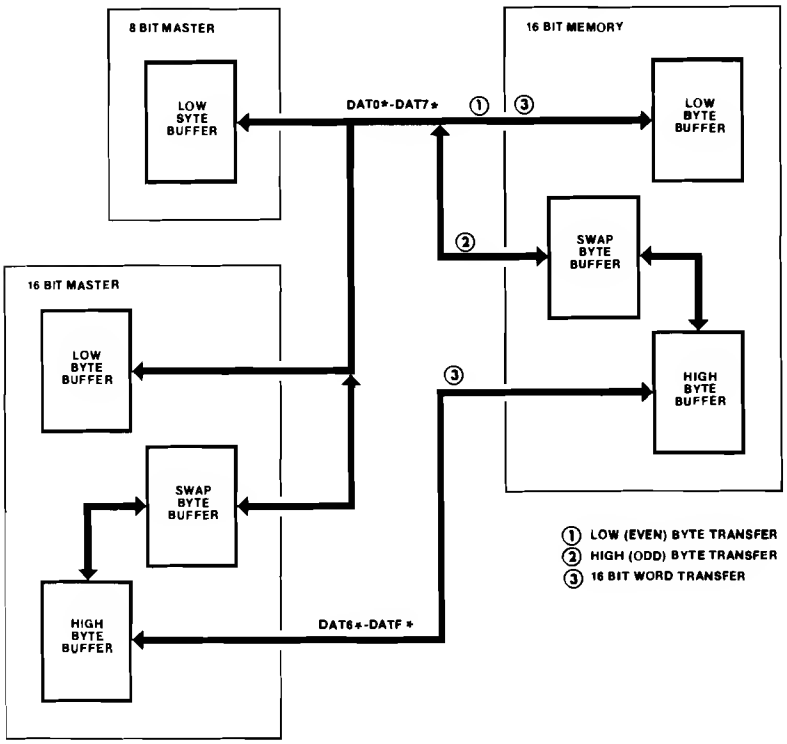


Fig. 6
796 Bus Data Line Usage

Two signals control the data transfers. Byte High Enable (BHEN*) active indicates that the bus is operating in the 16-bit mode, and the address bit 0(ADR0*) defines an even-byte or odd-byte transfer.

For an even byte transfer, BHEN* and ADR0* are inactive, indicating the transfer of an even byte. The transfer takes place across data lines DAT0*-DAT7*.

For an odd-byte transfer, BHEN* is inactive and ADR0* is active, indicating the transfer of an odd byte. On this type of transfer, the odd (high) byte is transferred through the Swap Byte Buffer to DAT0*-DAT7*. The high (odd) byte is transferred accross on DAT0*-DAT7* to make 8-bit and 16-bit systems compatible.

For a 16-bit transfer, BHEN* is active and ADR0* is inactive. On this type of transfer, the low (even) byte is transferred on DAT0*-DAT7* and the high (odd) byte is transferred across the bus on DAT8*-DATF*.

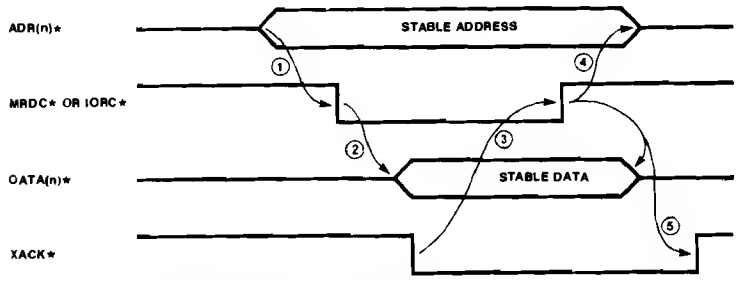
The 796 Bus data lines are always driven by three-state drivers.

2.2.2.5 *796 Bus Commands.* In this subsection we will discuss the command lines and how they work in conjunction with other lines to accomplish a read or a write operation. There are four command lines:

Function	Line
Memory Read Command	MRDC*
I/O Read Command	IORC*
Memory Write Command	MWTC*
I/O Write Command	IOWC*

The command lines, which are driven by three-state drivers on the bus master, indicate to the slave the action that is being requested.

2.2.2.5.1 *Read Operation.* The two read commands (MRDC* and IORC*) initiate the same basic type of operation. The only difference is that MRDC* indicates that the memory address is valid on the address lines, whereas IORC* indicates that the I/O port address is valid on the address lines. This address (memory or I/O port) must be valid on the bus 50 nanoseconds prior to the read command being generated. When the read command is generated, the slave module (memory or I/O port) places the data on the data lines and returns a Transfer Acknowledge (XACK*) signal, indicating that the data is on the bus. When the bus master receives the acknowledge, it strobes in the data and removes the command (MRDC* or IORC*) from the bus. The slave address (memory or I/O port) remains valid on the bus a minimum of 50 nanoseconds after the read command is removed. XACK* must be removed from the bus within 65 nanoseconds after the command is removed to allow for the next bus cycle. Fig. 7 shows the timing for the Memory Read or I/O Read command.

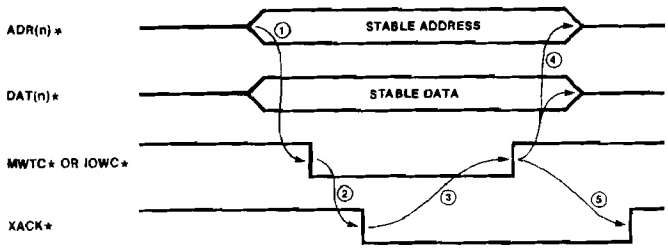


1. ADDRESS SETUP TIME: 50 NANOSECONDS MINIMUM.
2. TIME REQUIRED FOR SLAVE TO GET DATA ONTO BUS IN ACCORDANCE WITH SETUP TIME REQUIREMENT. XACK* CAN BE ASSERTED AS SOON AS DATA IS ON BUS.
3. TIME REQUIRED FOR MASTER TO REMOVE COMMAND.
4. ADDRESS AND DATA HOLD TIME: 50 NANOSECONDS MINIMUM.
5. XACK* AND DATA MUST BE REMOVED FROM THE BUS A MAXIMUM OF 65 NANOSECONDS AFTER THE COMMAND IS REMOVED.

Fig. 7
Memory or I/O Read Timing

2.2.2.5.2 *Write Operation.* The write commands (MWTC* and IOWC*) initiate the same basic type of operation. MWTC* indicates that the memory address is valid on the address lines, whereas IOWC* indicates that the I/O port address is valid on the address lines. The address (memory or I/O) and data must be valid on the bus 50 nanoseconds prior to the write command being generated. This requirement allows data to be latched on either the leading or trailing edge of the command. When the write command (MWTC* or IOWC*) is asserted, the data on the data lines is stable and can be accepted by the slave. The slave indicates acceptance of the data by returning a Transfer Acknowledge (XACK*), allowing the bus master to remove the command, address, and data from the bus, XACK* must be removed from the bus within 65 nanoseconds to allow for the next bus cycle. Fig. 8 shows the timing for the Memory Write or I/O Write command.

2.2.2.6 *Transfer Acknowledge (XACK*).* The Transfer Acknowledge (XACK*) signal is the response from the bus slave (memory or I/O) indicating that the commanded read or write operation is complete and that the data has been placed on, or accepted from, the data lines. In effect, this signal (XACK*) allows the bus master to complete the current bus cycle.



1 ADDRESS AND DATA SETUP; 50 NANOSECONDS MINIMUM.
2 TIME REQUIRED FOR SLAVE TO ACCEPT DATA.
3 TIME REQUIRED FOR MASTER TO REMOVE COMMAND FROM BUS.
4 ADDRESS AND DATA HOLD TIME; 50 NANOSECONDS MINIMUM.
5 XACK* MUST BE OFF THE BUS 65 NANOSECONDS AFTER COMMAND.

Fig. 8
Memory or I/O Write Timing

If a bus master addresses a non-existent or malfunctioning memory or I/O module, an acknowledge will not be returned to the master. If this should occur, the bus master would normally wait indefinitely for an acknowledge and would therefore never relinquish control of the 796 Bus. To avoid this possibility, a bus timeout function can optionally be implemented on a bus master to terminate a bus cycle after a preset interval, even if no acknowledge has been received. A bus timeout can therefore be defined as any data transfer cycle terminated by the master before the Transfer Acknowledge (XACK*) signal is received. The minimum allowable bus timeout interval is 1.0 millisecond.

2.2.2.7 *Inhibit (INH1* and INH2*).* The inhibit lines can be invoked for any memory read or memory write operation (MRDC* or MWTC*). An inhibit line is asserted by a slave to inhibit another slave's bus activity during a memory read or write operation. The inhibit signal generated by the inhibiting slave is derived from decoding the memory address lines (t_{ID} = 100 nanoseconds maximum). The inhibiting slave can decode a single address, a block of addresses, or any combination of single and block addresses.

When it detects the specific address during the actual command (MRDC* or MWTC*), the inhibiting slave generates an inhibit signal, which is sensed by the inhibited slave. When so inhibited, this slave module disables its drivers from all

data, address, and acknowledge bus lines, although it may actually perform internal operations. (All modules that may be inhibited must have completed internal operations with 1.5 microseconds from the start of the command line. This interval [1.5 microseconds] is also the minimum acknowledge (t_{ACC}) timing for modules issuing inhibits. This guarantees inhibited modules enough time to return to their normal state before the current bus command is completed.)

The slaves involved in the inhibit operation fall into three inhibit classes: top (inhibit) priority, middle priority, and bottom priority. In reference to the above paragraphs, a higher priority slave module would be the inhibiting slave and a lower priority slave would be the inhibited slave. INH1* is asserted (during the appropriate address) by a middle priority slave (such as a read-only memory module or memory-mapped I/O module) to inhibit the bus activity of a bottom priority slave (such as a read/write RAM module). INH2* is asserted (at the appropriate address) by a top priority slave (such as an auxiliary or a bootstrap ROM module) to inhibit the bus activity of a middle priority slave. The top priority slave shall also assert INH1* so that a bottom priority slave will also be inhibited. The inhibit lines shall be asserted low by open collector (or equivalent) drivers. When both a middle and a top priority inhibiting slave are activated, INH1* will be asserted by drivers on both modules.

The use of the inhibit signals during memory reads (MRDC*) shall not cause any adverse effects within the inhibited slave module. That is, data in the inhibited slave shall not be altered and its status register, if any, shall not be affected.

The use of the inhibit signals during memory writes (MWTC*) shall be allowed, and might or might not affect the data within the inhibited slave. If the data is affected, it shall be only within the one byte (or word) that is being addressed. (No other data within the inhibited slave shall be altered.)

The inhibit signals, when issued, shall be generated within 100 nanoseconds (t_{ID}) after the address is stable. (See Fig. 9.) A command may be generated as early as 50 nanoseconds (t_{AS}) after the address is stable. This timing can cause the inhibit to occur after the command has been received by the inhibited module. To prevent false acknowledges, modules that can be inhibited must not generate an acknowledge until the inhibit signals have had time to become valid (50 nanoseconds after the command).

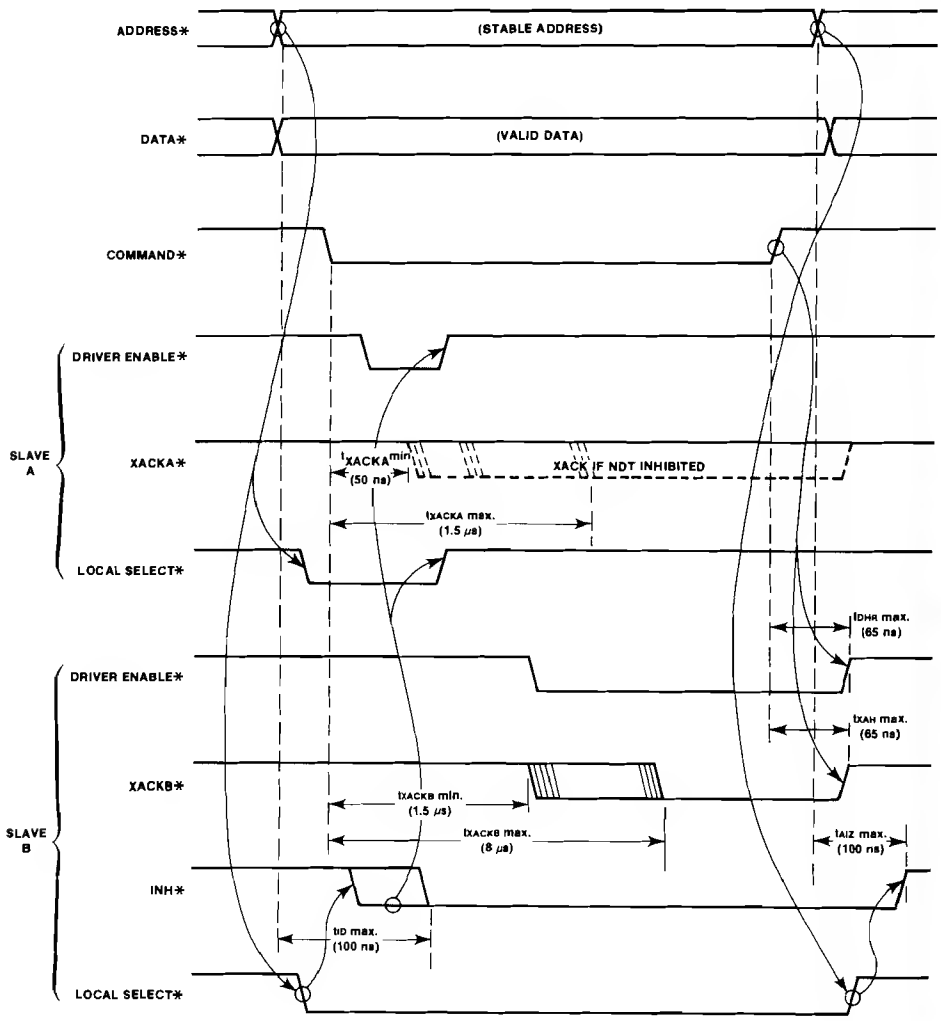


Fig. 9
Inhibit Timing for Write Operation

Fig. 9 shows the timing for an inhibit operation. In this example, both PROM and RAM have the same memory addresses; therefore, the PROM inhibits the RAM.

Although inhibit signals may be generated during IORC*, IOWC*, or INTA* operations, these signals are ignored by other slaves (including the slave that should respond to the INTA*, IORC*, or IOWC*).

2.2.2.8. *Lock (LOCK*).* The Lock line is driven by the master control of the bus when a locked bus access is required. A locked access is typically required in a read-modify-write semaphore operation to prevent another processor from accessing the memory between the read and the write. The busy line allows for this mutual exclusion on the 796 BUS. The Lock line allows mutual exclusion to be extended off of the bus. The Lock signal (LOCK*) must be active 100 nanoseconds prior to the read or write command going away. It must remain active a minimum of 100 nanoseconds after the falling edge of the command signal for the last locked memory cycle. The slave locks it multiple ported memory to the 796 bus when it is addressed and the lock line is asserted. The lock signal must not be asserted for more than 12 microseconds continuously. This assures the processor on the other side of the multiple ported memory that it will gain access to the memory in a reasonable amount of time. The busy signal (BUSY*) must be active whenever the Lock line is asserted. Fig. 11 shows the timing for the lock signal.

2.3 Interrupt Operations. The following subsections explain the 796 Bus signal lines used in the interrupt operation, and the two different types of interrupt implementation. Refer to Section 5.1.4 for information on levels of compliance with respect to interrupt attributes.

2.3.1 *Interrupt Signal Lines.*

2.3.1.1 *Interrupt Request Lines (INT0*-INT7*).* A set of interrupt request lines (INT0*-INT7*) is provided on the bus. An interrupt is generated by activating one of the eight interrupt request lines with an open-collector driver. All interrupts are level-triggered, rather than edge-triggered. Requiring no edge to trigger an interrupt allows several sources to be attached to each line. The interrupt request lines are prioritized, with INT0* having the highest priority and INT7* having the lowest priority.

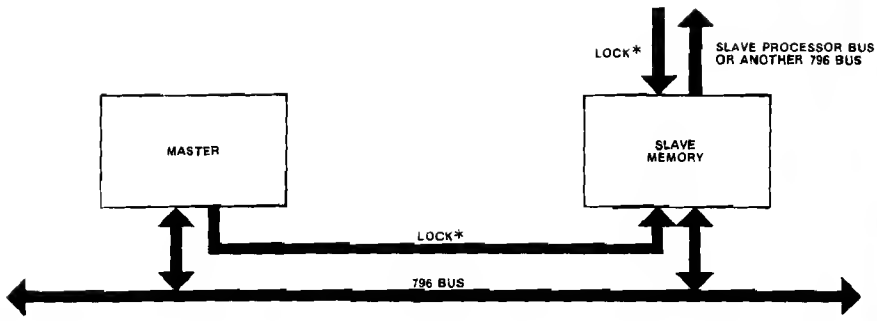


Fig. 10
796 Bus Lock Usage

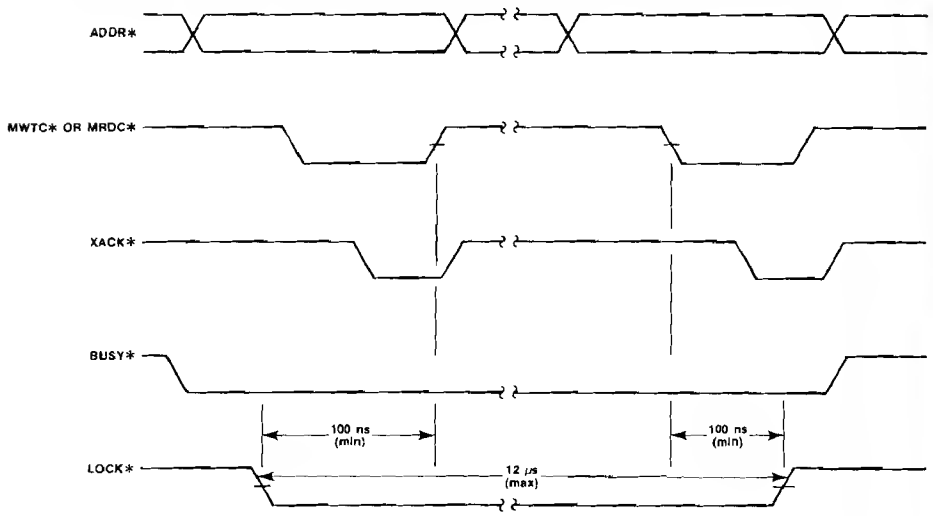


Fig. 11
Lock Timing

2.3.1.2 *Interrupt Acknowledge (INTA*).* An interrupt acknowledge line (INTA*), driven by the bus master, requests the transfer of interrupt information on the bus. The specific information timed onto the bus depends on the implementation of the interrupt scheme. In general, the leading edge of INTA* indicates that the address bus is active; the trailing edge indicates that data is present on the data lines.

2.3.2 *Classes of Interrupt Implementation.* There are two types of interrupt implementation schemes: Non-Bus Vectored (NBV) and Bus Vectored (BV). The two schemes are explained in the following subsections.

2.3.2.1 *Non-Bus Vectored Interrupts.* Non-Bus Vectored (NBV) interrupts are those interrupts handled on the bus master that do not require the 796 Bus for transfer of the interrupt vector address. The interrupt vector address is generated by the interrupt controller on the master and transferred to the processor over the local bus. The slave modules generating the interrupts can reside on the master module or on other bus modules, in which case they use the 796 Bus interrupt request lines (INT0*-INT7*) to generate their interrupt requests to the bus master. When an interrupt request line is activated, the bus master performs its own interrupt operation and process the interrupt. Fig. 12 shows an example of NBV interrupt implementation.

2.3.2.2 *Bus Vectored Interrupts.* Bus Vectored (BV) interrupts are those interrupts that transfer the interrupt vector address over the 796 Bus from the slave to the bus master using the INTA* command signal.

When an interrupt request occurs, the interrupt control logic on the bus master interrupts its processor. The processor on the bus master generates the INTA command, freezing the state of the interrupt logic for priority resolution. The bus master also overrides (retains the bus between bus cycles) the 796 Bus to guarantee itself back-to-back bus cycles. After the first INTA* command, the bus master's interrupt control logic puts an interrupt code on the 796 Bus address lines. The interrupt code is the address of the highest priority active interrupt request line. At this point in the BV interrupt procedure, two different sequences can occur because the 796 Bus can support masters that generate either two or three INTA* commands.

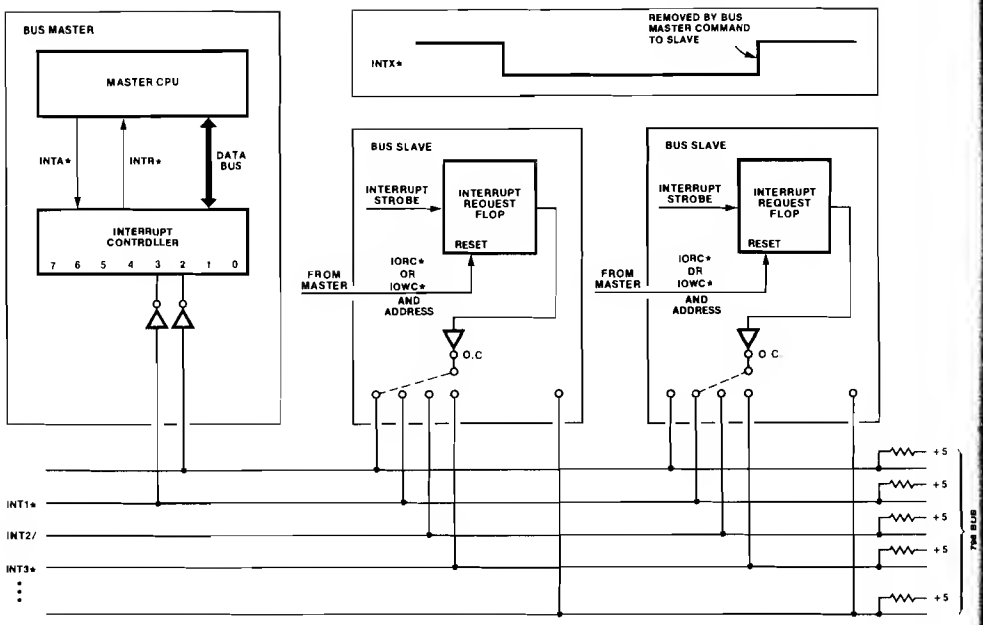


Fig. 12
Non-Bus Vectored (NBV) Interrupt Logic

If the bus master generates two INTA* commands, one more INTA* command will be generated. This second INTA* causes the bus slave interrupt control logic to transmit its interrupt vector address on the 796 Bus data lines. The address is used by the bus master to service the interrupt.

If the bus master generates three INTA* commands, two more INTA* commands will be generated. These two INTA* commands allow the bus slave to put its 2-byte interrupt vector address on the 796 Bus data lines (one byte for each INTA*). The interrupt vector address is used by the bus master to service the interrupt.

NOTE

The 796 Bus can support only one type of Bus Vectored interrupt in a given system. However, the 796 Bus can support both Bus Vectored (BV) and Non-Bus Vectored (NBV) interrupts within the same system.

Fig. 13 depicts an example of BV Interrupt implementation.

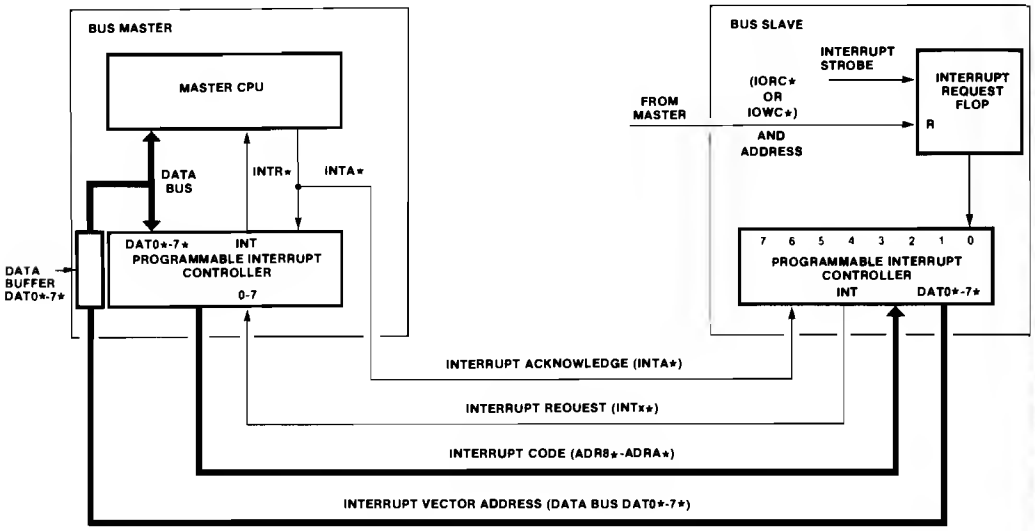
2.4 796 Bus Exchange. The 796 Bus can accommodate several bus masters on the same system, each taking control of the bus as it needs to effect data transfers. The bus masters request bus control through a bus exchange sequence.

The discussion of the 796 Bus exchange will be separated into three parts. The first part explains the signals involved, the second part discusses the bus exchange priority techniques (serial and parallel), and the third part explains the implementation of the exchange logic.

2.4.1 *796 Bus Exchange Signals.* A set of six signals is uesd to implement the bus exchange operation. All bus exchange signals are synchronized by BCLK*.

2.4.1.1 *Bus Clock (BCLK*).* This periodic clock signal is used to synchronize the exchange logic, with synchronization occuring on the trailing (high-to-low) edge of the pulse. BCLK* has a duty cycle of approximately 50 percent, a maximum frequency of 10 MHz, and can be slowed, stepped, or stopped as called for by system design. There is no requirement for synchronization between BCLK* and CCLK*, but they may be derived from the same source. The BCLK* line is driven by a TTL clock driver.

2.4.1.2 *Bus Busy (BUSY*).* This signal is driven by the master in control of the bus. All other masters monitor BUSY* to determine the state of the bus. This bidirectional signal, which is driven by an open-collector gate, is synchronized by BCLK*.



TIMING

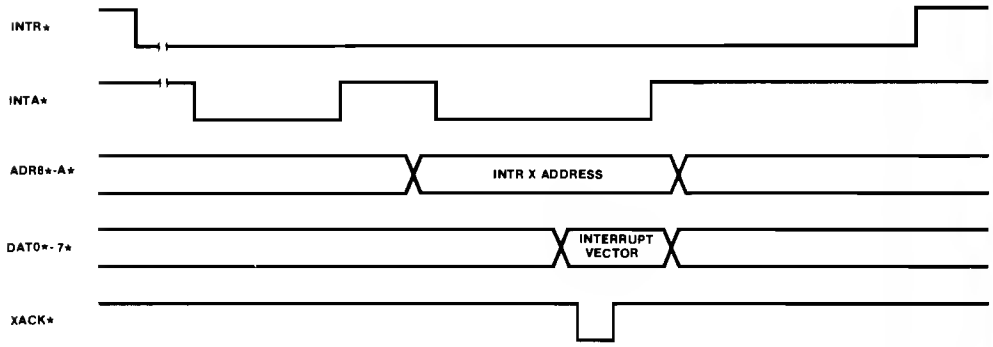


Fig. 13
Bus Vectored (BV) Interrupt Logic

2.4.1.3 *Bus Priority In (BPRN*).* A non-bused signal that indicates to a master that no master of higher priority is requesting control of the bus. BPRN* is synchronized by BCLK* and driven by TTL gates. In a serial resolution scheme, this is the master's input from the priority chain. In a parallel resolution scheme, this is the master's input from the parallel priority circuit.

2.4.1.4 *Bus Priority Out (BPRO*).* This non-bused signal, when activated by a bus master, indicates to the bus master of the next lower priority that it may gain control of the bus (i.e., no higher priority requests are pending for control of the bus). This signal is used only in a daisy-chained serial priority resolution scheme and should be connected to the Bus Priority In (BPRN*) input of the next lower priority bus master. BPRO* is driven by TTL gates and is synchronized by BCLK*.

NOTE

Each bus master must allow its BPRO* signal to be disconnected from the BPRO* line on the 796 Bus so that, if desired, a parallel priority resolution scheme can be used. This capability is to allow some bus masters to have their BPRN* inputs driven by a central parallel resolution circuit instead of by the BPRO* of the next higher priority master.

2.4.1.5 *Bus Request (BREQ*).* The Bus Request (BREQ*) line is used with the parallel priority resolution scheme, and is a request of the master for 796 Bus control. The priorities of the BREQ* from each master are resolved in a parallel priority resolution circuit. The highest priority request enables the BPRN* input of that master, allowing it to gain control of the bus. BREQ* is synchronized by BCLK* and is a TTL output.

2.4.1.6 *Common Bus Request (CBRQ*) (Optional).* Any master that wants control of the 796 Bus but does not control it, can activate CBRQ* with an open-collector gate. If CBRQ* is high, it indicates to the bus master that no other master is requesting the bus and therefore the present bus master can retain the bus. There are times when this can save the bus exchange overhead for the current master. This is

because quite often when a master is controlling the bus, there are no other masters that are requesting the bus. Without CBRQ*, only BPRN* indicates whether or not another master is requesting the bus and, for BPRN*, only if the other master is of higher priority. Between the master's bus transfer cycles, in order to allow lower priority masters to take the bus if they need it, the master must give up the bus. At the start of the master's next transfer cycle, the bus must be regained. If no other master has the bus, this can take approximately three BCLK* periods. To avoid this overhead of unnecessarily giving up and regaining the bus when no other masters need it, CBRQ* may be used. Any master that wants but does not have the bus, must drive this line low (true). The master that has the bus can, at the end of a transfer cycle, sense CBRQ*. If it is not low, then the bus does not have to be released, thereby eliminating the delay of regaining the bus at the start of the next cycle. (At any time before the master's next cycle, any other master desiring the bus will drive CBRQ* and cause the master to relinquish the bus at that time.)

Masters that use CBRQ* must be able to disable that function such that they can be used with masters that do not generate the CBRQ* signal.

2.4.2 *Bus Exchange Priority Techniques.* Two bus exchange priority techniques are discussed: a serial technique and a parallel technique. Fig. 14 and Fig. 15 illustrate these two techniques. Note that the parallel and serial schemes are compatible and therefore can be combined and used together on the same bus. The bus exchange implementation discussed in 2.4.3 is the same for both techniques.

2.4.2.1 *Serial priority Technique.* Serial priority resolution is accomplished with a daisy-chain technique (see Fig. 14). With such a scheme, the bus priority output (BPRO*) of each master is connected to the bus priority input (BPRN*) of the next lower priority master. The BPRN* of the highest priority master in the serial chain shall either be always active or connected to a central Bus Arbiter as described in 2.4.2.2. The latter connection would be used if a parallel-serial priority structure were used.

Serial priority resolution is accomplished in the following manner. The BPRO* output for a particular master is asserted if and only if its BPRN* input is active and that master is not requesting control of the bus. Thus, if a master requests control of the bus, it shall set its BPRO* high, which in turn disables the BPRN* of all lower

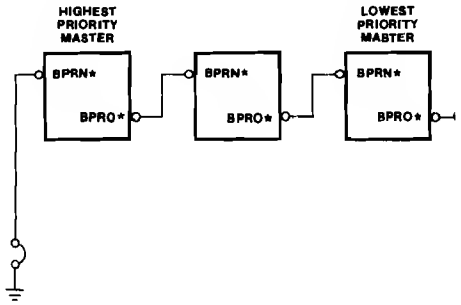


Fig. 14
Serial Priority Technique

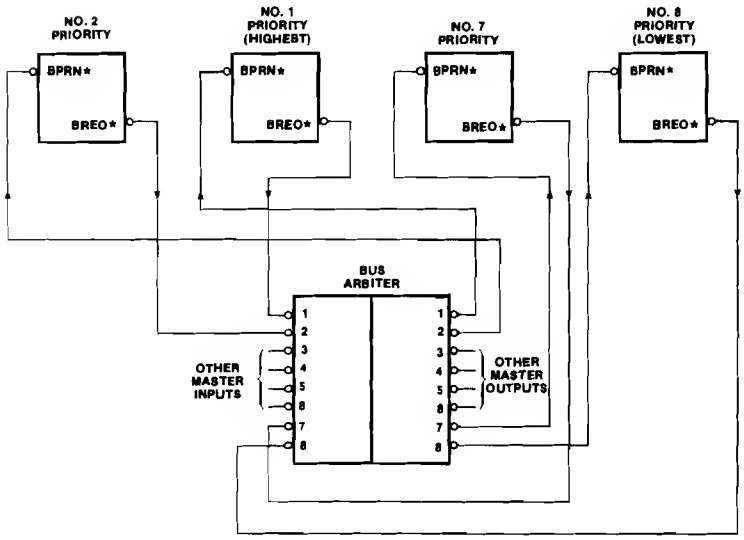


Fig. 15
Parallel Priority Technique

priority masters. The number of masters that can be linked in a serial chain is limited by the fact that the BPRN* signal must propagate through the entire chain within one BCLK* cycle. If the maximum BCLK* of 10 MHz is used, then the number of masters in a serial chain is limited to three.

2.4.2.2 *Parallel Arbitration Technique.* In the parallel technique, the bus allocation is determined by a Bus Arbiter (see Fig. 15). This may be a priority scheme, which determines the next master by a fixed priority structure or some other mechanism for allocation (e.g., sequential). The BREQ* lines are used by the arbiter to signal the next master on the appropriate BPRN* line. The BPRO* lines are not used in the parallel allocation BPRN* scheme.

3. Electrical Specifications

This section presents the electrical specifications for the 796 Bus as follows:

(1) General bus considerations of the state relationships, signal line characteristics, and power supplies

(2) Timing specifications for the bus signals

(3) Specifications for the signal line drivers and receivers, as well as the electrical termination requirements

When electrical specifications indicate minimum or maximum values for the bus, they must be measurable at any point on the bus.

Note that a particular implemented bus could have any amount of bus propagation delay and ringing (before setup times), as long as all bus parameters (e.g., setup, hold, and other times) are met at all points on the bus. However, to facilitate the design of a compatible set of modules (masters and slaves) that use the bus, the standard maximum bus propagation delay will be specified as t_{PD} (max).

3.1 General Bus Considerations.

3.1.1 *Logical and Electrical State Relationships.* The signal names indicate whether or not the signal lines on the 796 Bus are active high or active low. If the signal name ends with a nathan (" * ", a non-superscript asterisk), then the signal is active low and its logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	H=TTL high state	$5.25V \geq H \geq 2.0V$	$5.25V \geq H \geq 2.4V$
1	L=TTL Low state	$.8V \geq L \geq -.5V$	$.5V \geq L \geq 0V$

If the signal name has no nathan (no " * "), then the signal is active high and its logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	L=TTL low state	.8V ≥ L ≥ −.5V	.5V ≥ L ≥ 0V
1	H=TTL high state	5.25V ≥ H ≥ 2.0V	5.25V ≥ H ≥ 2.4V

These specifications are based on TTL, where the power source is 5V ±5%, referenced to logic ground (GND).

When specified, current flow into a node has a positive sign and current flow out of a node has a negative sign.

3.1.2 *Signal Line Characteristics.* The following subsections describe two types of requirements. The first includes the requirements on the signal line that are measured when the signal line is in use. The second type includes those that are measured under special test conditions.

3.1.2.1 *In-Use Signal Line Requirements.* During normal use, the rise and fall times of the signals depend on which type of driver is used (see 3.3). Typical rise and fall times are:

	Open Collector	Totem Pole	3-State
Rise Time	—	10 ns	10 ns
Fall Time	10 ns	10 ns	10 ns

The maximum signal propagation delay on the bus is t_{PD} (max). This is measured from the edge of any one board plugged into the 796 Bus to any other board plugged into the 796 Bus:

$$t_{PD} \text{ (max)} = 3 \text{ ns}$$

These dynamic signal parameters can be tested by using 74S20 gates as drivers.

NOTE

For all boards plugged into the bus, the setup, hold, and any other times are measured at the edge of the board where it is plugged into the bus. This means that all board-internal delays must be taken into account, while still providing for the setup, hold, and other times.

After Power-Up, the following specifications apply:

(1) Bus termination required for each signal line (see 3.3).

(2) Settling time for all command line signals (see 2.2.2.5) after a transition is zero. On these lines the ringing cannot go beyond the noise immunity levels—i.e., high, minimum; or low, maximum. This also applies to the Transfer Acknowledge and Inhibit lines.

For all address lines (see 2.2.2.3) the signals must be stable (settled) at least 50 nanoseconds before any command line goes active (setup time). This settling requirement means there can be no ringing beyond the noise immunity levels (high, minimum; low, maximum). These requirements also apply to the data lines (see 2.2.2.4) during any write operations.

For all data lines during read operations, the setup time is zero before the Transfer Acknowledge (XACK *) signal goes active; and the hold time is zero after the read-type command goes inactive.

The setup, hold, and command ringing are summarized and graphically presented in Fig. 16.

3.1.2.2 *Backplane Signal Trace Characteristics.* Requirements for line-to-line coupling characteristics are shown in Fig. 17. The specific test conditions under which the specifications are to be met are also shown.

3.1.3 *Power Supply Specifications.* Table 1 provides all power supply specifications. All voltages not shown in Table 1 that may be required on a board plugging into the 796 Bus should be derived from one of the standard voltages (+5V, +12V, −12V).

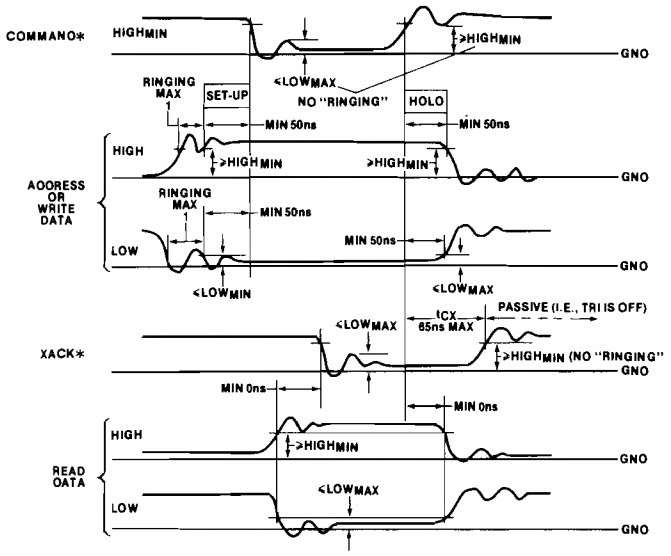


Fig. 16
Setup, Hold, and Command Ringing Summary

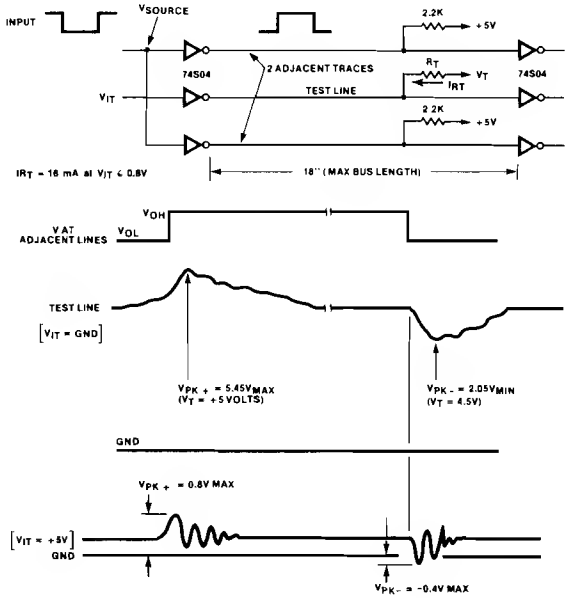


Fig. 17
Line-to-Line Coupling Characteristics

Table 1
796 Bus Power Supply Specifications

	Standard[1]			
Parameter	Ground	+5	+12	−12
Mnemonic	GND	+5V	+12V	−12V
Bus Pins	P1-1,2,11,12, 75,76,85,86	P1-3,4,5,6, 81,82,83, 84	P1-7,8	P1-79,80
Tolerance	Ref.	±1%	±1%	±1%
Combined Line & Load Reg	Ref.	0.1%	0.1%	0.1%
Ripple (Peak to Peak)	Ref.	50 mV	50 mV	50 mV
Transient Response (50% Load Change)		100 μs	100 μs	100 μs

[1]Point of measurement is at connection point between motherboard and power supply. At any card edge connector a degradation of 2% maximum (e.g. voltage tolerance ±2%) is allowed.

3.1.4 *Temperature and Humidity.* Bus specifications should be met with temperature and humidity within the following ranges:

Temperature: 0-55 °C (32-150 °F); freemoving air across modules and bus

Relative Humidity: 90% maximum (no condensation)

This represents standard environment for the 796 Bus. It may be desirable to create more (or less) severe environmental restrictions in some applications.

3.2 **Timing**. This subsection describes all timing specifications on the 796 Bus. It does not present descriptions or functional relationships (which are given in Section 2); however, this section does imply the functionality when relating two signals.

Table 2 summarizes the timing specifications in this section. For detailed descriptions, refer to the specific subsection(s) in the right-hand column.

The timing diagrams shown in this section usually show the minimum or maximum values required for each parameter. However, for clarity, the diagrams in this specification do not usually show both the minimum and maximum parameters. For this reason, the bus timing specification (Table 2) should be referenced for complete information. The timing diagrams show how all of the parameters are defined in relation to the signals involved.

Table 2
796 Bus Timing Specifications Summary

Parameter	Description	Minimum	Maximum	Units	Reference
t_{AH}	Address Hold Time	50		ns	3.2.1, 3.2.2, 3.2.4
t_{AIZ}	Address to Inhibit High Delay	0	100	ns	3.2.3
t_{AS}	Address Setup Time (at slave board)	50		ns	3.2.1, 3.2.2, 3.2.4
t_{BCY}	BCLK* Period	100	∞	ns	3.2.5
t_{BPRNO}	BPRN* to BPRO*	0	30	ns	3.2.5
t_{BPRNS}	BPRN* to ↓BCLK* Setup Time	22		ns	3.2.5
t_{BPRO}	↓BCLK* to BPRO*	0	40	ns	3.2.5
t_{BREQH}	↓BLCK* to BREQ* High Delay	0	35	ns	3.2.5
t_{BREQL}	↓BCLK* to BREQ* Low Delay	0	35	ns	3.2.5
t_{BSYO}	CBRQ*●BUSY* to ↓BUSY	—	12	μs	3.2.5
t_{BUSY}	BUSY* delay from ↓BCLK*	0	70	ns	3.2.5
t_{BUSYS}	BUSY* to ↓BCLK Setup Time	25		ns	3.2.5
t_{BW}	BCLK* Width	$0.35t_{BCY}$	$0.65t_{BCY}$		3.2.5
t_{CBRO}	↓BCLK* to CBRQ*	0	60	ns	3.2.5
t_{CBRQS}	CBRQ* to ↓BCLK* Setup Time	35		ns	3.2.5
t_{CCY}	CCLK* Period	100	110	ns	3.2.6
t_{CMD}	Command Pulse Width	100	t_{TOUT}	ns	3.2.1, 3.2.2
t_{CMPH}	Command Hold Time	20		ns	3.2.1, 3.2.2
t_{CPM}	Central Priority Module Resolution Delay (parallel priority)	0	$t_{BCY}-t_{BREQ}-2t_{PD}-t_{BPRNS}-t_{SKEW}$		3.2.5
t_{CSEP}	Command Separation	100		ns	3.2.4, 3.2.6
t_{CW}	CCLK* Width	$0.35t_{CCY}$	$0.65t_{CCY}$	ns	3.2.6
t_{DHR}	Read Data Hold Time	0	65	ns	3.2.1, 3.2.4
t_{DHW}	Write Data Hold Time	50		ns	3.2.2
t_{DS}	Write Data Setup Time	50		ns	3.2.2

Table 2
796 Bus Timing Specifications Summary (Cont'd.)

Parameter	Description	Minimum	Maximum	Units	Reference
t_{DXL}	Read Data Setup Time to XACK*	0		ns	3.2.1, 3.2.4
t_{IAD}	XACK* Disable from Inhibit (internal parameter on an inhibited slave; used to determine t_{XACKA} min.)	0	100 (arbitrary)	ns	2.3.2
t_{ID}	Inhibit Delay	0	100 (recommend <100 ns)	ns	3.2.3
t_{INIT}	INIT* Width	5		ms	3.2.6, 3.2.7
t_{INTA}	INTA* Width	250		ns	3.2.4
t_{LCKH}	LOCK* hold time from command active	100		ns	3.2.6
t_{LCKS}	LOCK* to command setup time	100		ns	3.2.6
t_{LOCK}	LOCK* Width		12	μs	3.2.6
t_{OUT}	Timeout Delay	1	dc (∞)	ms	—
t_{PD}	Standard Bus Propagation Delay		3	ns	3.1.2, 3.2.5
t_{SKEW}	BCLK* Skew		t_{PD}		3.2.5
t_{XACK}	XACK* Time (for slaves without inhibit function)	0	8	μs	3.2.1, 3.2.2, 3.2.4
t_{XACKA}	XACK* Time of an Inhibited Slave	t_{IAD} +50 ns	1500	ns	3.2.3
t_{XACKB}	XACK* Time of an Inhibiting Slave	1500	8000	ns	3.2.3
t_{XAH}	XACK* Hold Time	0	65	ns	3.2.1, 3.2.2, 3.2.4
Serial Priority	See 3.2.5				

3.2.1 *Read Operations (I/O and Memory).* A read operation transfers data from memory or from I/O to the master that is controlling the bus (see 2.2.). The lines involved and timing specifications for a read operation are shown in Fig. 18. See the special inhibit oepration in 3.2.3.

3.2.2 *Write Operations (I/O and Memory).* A write operation transfers data from the master controlling the bus to memory or I/O (see 2.2.). Timing for a write operation is shown in Fig. 19. See 3.2.3 for inhibit operations.

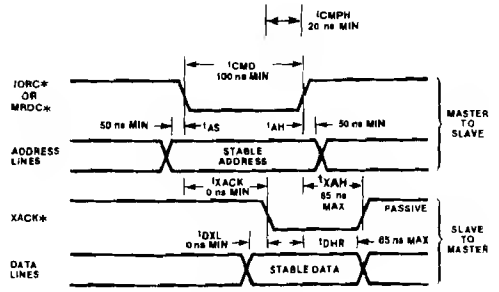


Fig. 18
Read AC Timing

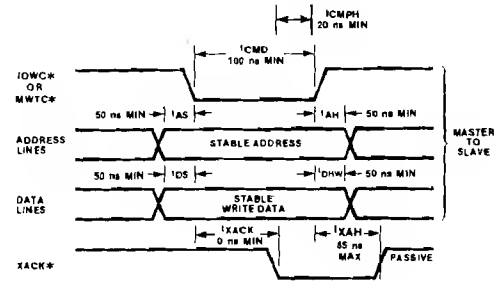


Fig. 19
Write AC Timing

3.2.3 *Inhibit Operations.* An inhibit operation may accompany any memory read or memory write operation. The main effect is for one slave to inhibit another slave from driving the data lines and from returning (driving) an acknowledge (XACK*). I/O addresses cannot be inhibited. Although inhibit signals may be generated during IORC*, IOWC*, or INTA* operations, these signals are ignored by other slaves (including the slave that should respond to the INTA*, IORC*, or IOWC*). Inhibit timing is as illustrated in Fig. 20. Related subsections are:

Subsection	Number
Functional Descriptions	2.1.3.2.3
Timing Specification Summary	3.2
Read Operations	3.2.1
Write Operations	3.2.2
Interrupt Implementations	3.2.4

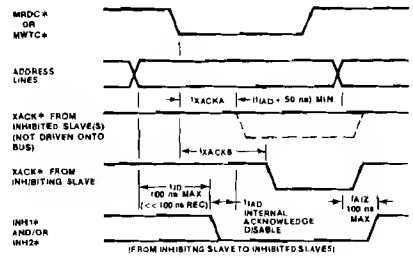


Fig. 20
Inhibit AC Timing

3.2.4 *Interrupt Implementations.* There are two types of interrupt implementation schemes: Non-Bus Vectored (NBV) and Bus Vectored (BV).

3.2.4.1 *NBV Interrupts.* NBV interrupts are handled on the bus master and do not require the 796 Bus for transfer of an interrupt vector address. The slave modules generating the interrupts may reside on the master module or on other bus modules, in which case they use the 796 Bus interrupt request lines (INT0 * -INT7 *) to generate interrupt requests to the bus master. When an interrupt request line is activated, the bus master performs its own internal interrupt operations and then processes the interrupt.

3.2.4.2 *BV Interrupts.* BV interrupts are those interrupts that transfer the interrupt vector address along the 796 Bus from the slave to the bus master in response to the INTA* command signal. BV interrupt timing is shown in Fig. 21.

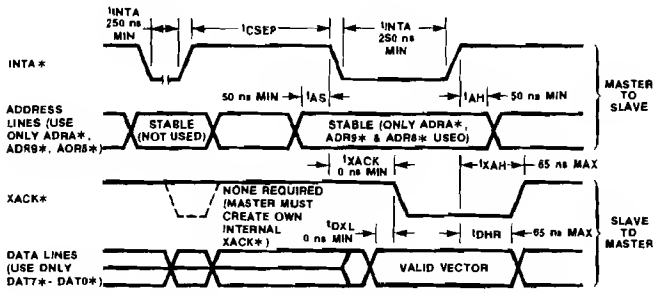


Fig. 21
Bus Vectored (BV) Interrupt AC Timing

When an interrupt request occurs, the interrupt control logic on the bus master interrupts its processor. The processor on the bus master generates an INTA* command, which freezes the state of the interrupt logic on the 796 Bus for priority resolution. The bus master also locks the 796 Bus (retains the bus between bus cycles) to guarantee itself back-to-back bus cycles. After the first INTA* command, the bus master's interrupt control logic puts an interrupt code onto the 796 Bus address lines. The interrupt code is the address of the highest priority active interrupt request line. At this point in the BV interrupt procedure, two different sequences could take place. The difference occurs because the 796 Bus can support masters that generate either two or three INTA* commands during the interrupt process.

If the bus master generates two INTA* commands, one more INTA* command will be generated. This second INTA* causes the bus slave interrupt control logic to transmit its interrupt vector address on the 796 Bus data lines. The address is used by the bus master to service the interrupt.

If the bus master generates three INTA* commands, two more INTA* commands will be generated. These two INTA* commands allow the bus slave to put its 2-byte interrupt vector address onto the data lines (one byte for each INTA* command). The interrupt vector address is used by the bus master to service the interrupt.

NOTE

The 796 Bus can support only one type of BV interrupt in a given system. However, it can support both BV and NBV interrupts in the same system.

Subsections related to BV and NBV interrupts are:

Subsection	Number
Functional Descriptions	2.3.2.2
Timing Specification Summary	3.2

3.2.5 *Bus Control Exchanges.* A bus control exchange takes control of the bus (i.e., the ability to do read, write, and interrupt acknowledge operations) from one master and gives it to another master. See 2.4 for a functional description of this process.

For a master that does not use the bus signal CBRQ* (Common Bus Request), the timing specifications in Fig. 22 apply.

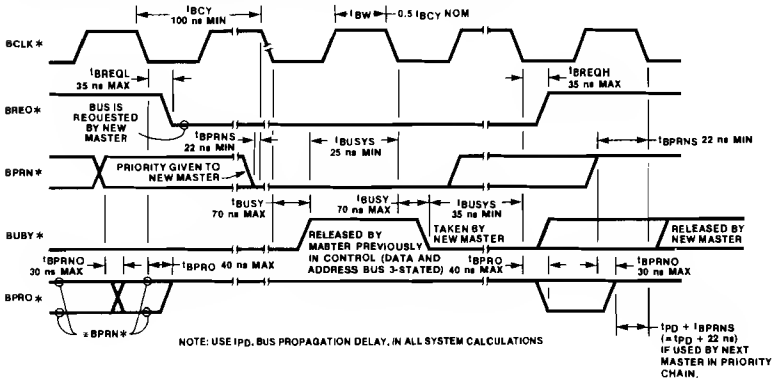


Fig. 22
Bus Exchange AC Timing

For a system using CBRQ* (Common Bus Request), each master must also satisfy the timing requirements illustrated in Fig. 23. Note that before "releasing the bus" (i.e., releasing BUSY*), the hold times, etc., of any ending cycle must still be met as described in the previous subsections of this chapter. Likewise, after "taking the bus" (i.e., driving BUSY* low), it is necessary to satisfy all applicable setup and other timing parameters for a cycle just beginning.

3.2.5.1 *Serial Priority.* For a system that uses a serial priority scheme (i.e., daisy-chain BPRO*s to BPRN*s) (see 2.4), the timing specifications in Fig. 24 apply.

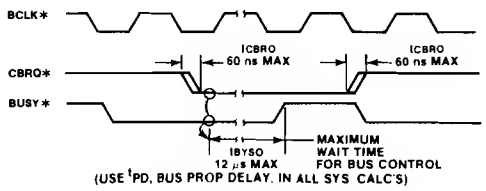


Fig. 23
Common Bus Request AC Timing

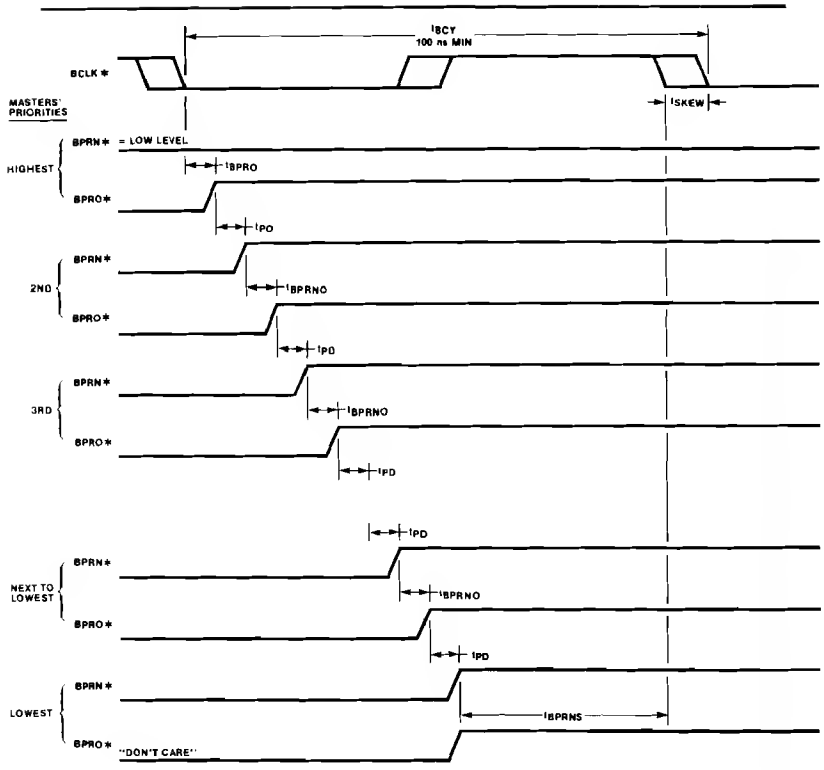


Fig. 24
Serial Priority AC Timing

3.2.5.2 *Parallel Priority.* For a system that uses a parallel priority scheme (i.e., a central priority resolver) (see 2.4), the following system and CPM (Central Priority Module) timing specifications of Fig. 25 apply.

3.2.6 *Miscellaneous Timing.* The timing diagrams in Figs. 26, 27, 28, and 29 show the timing of Constant Clock (CCLK*), Command Separation (t_{CSEP}), Initialize (t_{INIT}), and Lock (LOCK*), respectively.

3.3 Receivers, Drivers and Terminations. Non-timing specifications unique to each signal line or to groups of signal lines are presented in Table 3. The requirements for the signal line receivers, drivers, and bus terminations, and the locations of the receiver, driver, and termination for each signal are given.

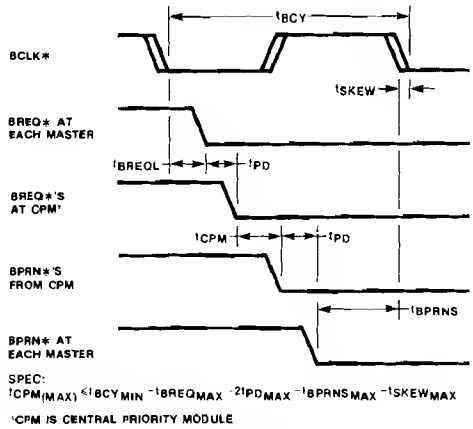


Fig. 25
Parallel Priority AC Timing

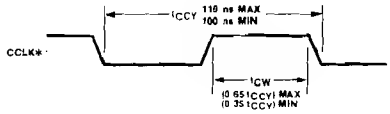


Fig. 26
Constant Clock AC Timing

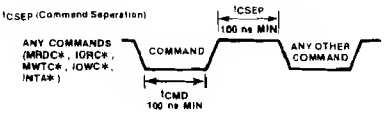


Fig. 27
Command Separation AC Timing

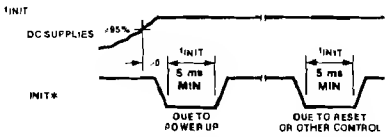


Fig. 28
Initialize AC Timing

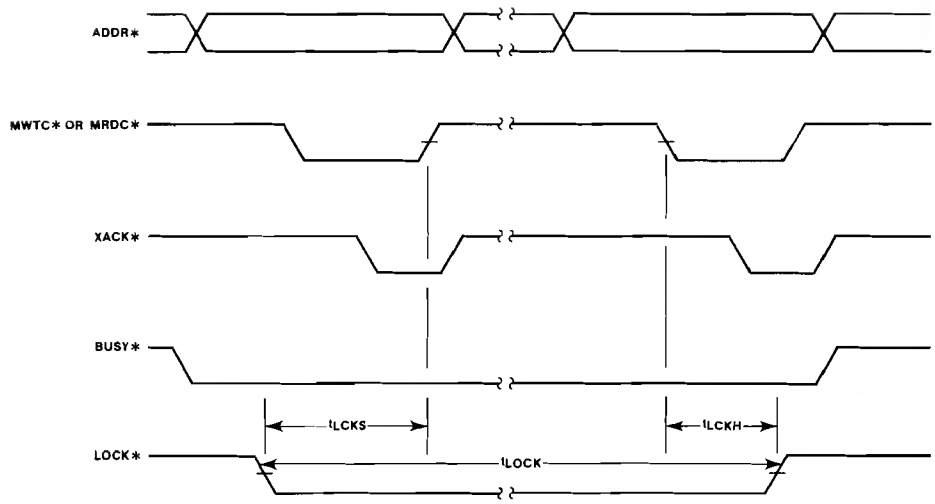


Fig. 29
Lock AC Timing

Table 3
Bus Drivers, Receivers, and Terminations

	Driver[1,3]						Receiver[2,3]				Termination			
Bus Signals	Location	Type	I_{OL} Min_{mA}	I_{OH} $Min_{\mu a}$	I_{OH} $Max_{\mu a}$	C_O Min_{pf}	Location	I_{IL} Max_{mA}	I_{IH} $Max_{\mu a}$	C_I Max_{pf}	Location[5]	Type	R	Units
DAT0* - DATF* (16 lines)	Masters & Slaves	TRI	16	-2000	—	300	Masters & Slaves	-0.8	125	18	1 place	Pullup	2.2	KΩ
ADR0* - ADR17*, BHEN* (25 lines)	Masters	TRI	16	-2000	—	300	Slaves	-0.8	125	18	1 place	Pullup	2.2	KΩ
MRDC*, MWTC*	Masters	TRI	32	-2000	—	300	Slaves (Memory; Memory-Mapped I/O)	-2	125	18	1 place	Pullup	1	KΩ
IORC*, IOWC*	Masters	TRI	32	-2000	—	300	Slaves (I/O)	-2	125	18	1 place	Pullup	1	KΩ
XACK*	Slaves	TRI	32	-400	—	300	Masters	-2	125	18	1 place	Pullup	510	Ω
INH1*, INH2*	Inhibiting Slaves	OC	16	—	-250	300	Inhibited Slaves (RAM, PROM, ROM, Memory-Mapped I/O)	-2	50	18	1 place	Pullup	1	KΩ
BCLK*	1 place (Master usually)	TTL	48	-3000	—	300	Masters	-2	125	18	Motherboard	To +5V To GND	220 330	Ω Ω
BREQ*	Each Master	TTL	10	-200	—	60	Central Priority Module	-2	50	18	Central Priority Module (not req)	Pullup	1	KΩ
BPRO*	Each Master	TTL	3.2	-200	—	60	Next Master in Serial Priority Chain at its BPRN*	-1.6	50	18	(not req)			
BPRN*	Parallel: Central Priority Module Serial: Prev Masters BPRO*	TTL	16	-400	—	300	Masters	-4	100	18	(not req)			

Table 3
Bus Drivers, Receivers, and Terminations (Cont'd.)

			Driver[1,3]					Receiver[2,3]				Termination		
Bus Signals	Location	Type	I_{OL} Min_{mA}	I_{OH} $Min_{\mu a}$	I_{OH} $Max_{\mu a}$	C_O Min_{pf}	Location	I_{IL} Max_{mA}	I_{IH} $Max_{\mu a}$	C_I Max_{pf}	Location[5]	Type	R	Units
LOCK*	Master	TRI	32	-2000	—	300	All	-2	125	18	1 place	Pullup	1	KΩ
BUSY*, CBRQ*	All Masters	OC	20	—	-250	300	All Masters	-2	50	18	1 place	Pullup	1	KΩ
INIT*	Master	OC	32	—	-250	300	All	-2	50	18	1 place	Pullup	2.2	KΩ
CCLK*	1 place	TTL	48	-3000	—	300	Any	-2	125	18	Mother-board	To +5V	220	Ω
												To GND	330	Ω
INTA*	Masters	TRI	32	-2000	—	300	Slaves (Interrupting I/O)	-2	125	18	1 place	Pullup	1	KΩ
INT0* - INT7* (8 lines)	Slaves	OC	16	—	-250	300	Masters	-1.6	40	18	1 place	Pullup	1	KΩ

[1] Driver Requirements:
- I_{OH} = High Output Current Drive
- I_{OL} = Low Output Current Drive
- C_O = Capacitance Drive Capability
- TRI = 3-State Drive
- OC = Open Collector Driver
- TTL = Totem-pole Driver

[2] Receiver Requirements:
- I_{IH} = High Input Current Load
- I_{IL} = Low Input Current Load
- C_I = Capacitive Load

[3] For low and high voltage specifications see 3.1.1.

[4] ±5%, ¼W Resistors

[5] All termination resistors specified as "1 place" are typically located on the motherboard.

4. Mechanical Specifications

This section describes all the physical and mechanical specifications that a designer must be concerned with when designing a 796 Bus backplane or when designing printed circuit boards that will plug into the 796 Bus interface.

4.1 Backplane Considerations. This section is a discussion of the things that the designer must consider when designing a 796 Bus backplane.

The maximum length of the backplane connecting modules is 18 inches. Extender boards used within the system will not be supported by the bus unless the overall resulting length of the bus including the extender card is less than the 18-inch maximum.

4.1.1 *Board to Board Relationships.* The following printed circuit board specifications must be adhered to when designing 796 Bus compatible boards which are to operate in a 0.6-inch board to board spacing backplane.

a. *Board to Board Spacing (L_C)* — center to center of boards when plugged into backplane must be at least 0.6 inches ±0.02.

b. *Board Thickness (L_T)* — the typical board thickness is 0.062 ±0.005 inches.

c. *Component Lead Length (L_L)* — the length of the component leads below the printed circuit board cannot exceed 0.093 inches.

d. *Component Height (L_H)* — the following equation is used to determine the maximum height of the components above the printed circuit board:

$$L_H < L_C - L_T - L_L$$

$$L_H < 0.58" - 0.067" - 0.093"$$

$L_H < 0.420$ inches (including board warpage)

Electrically conductive components require L_H to be decreased to 0.40 inches.

An example of a typical backplane and the components necessary to implement it are shown in Fig. 31.

This section contains only the mechanical specifications for designing a 796 Bus interface. The designer must also take into consideration the electrical specifications in Section 3.

4.1.2 *796 Bus Pin Assignments.* Printed circuit boards which are designed to interface to the 796 Bus have two connectors which plug into the backplane. P1 (Primary) and P2 (Auxiliary). Table 4 shows the pin/signal assignments for the P1 connector on the printed circuit boards. Reserved signals on the P1 connector must be bussed as normal signal lines on the backplane. Table 5 shows the pin/signal assignments for the P2 connector on the printed circuit boards. If a backplane is used then the "Reserved and bussed" signals must be bussed as normal signal lines, and the "Reserved but not bussed" signals shall have no connections.

4.2 796 Bus Board Form Factors. Certain 796 Bus characteristics must be taken into consideration when designing printed circuit boards that interface to it. The designer will ensure himself of 796 Bus compatibility if the specifications discussed in this chapter are followed.

4.2.1 *Connector Naming and Pin Numbering Standards.* The connectors on the printed circuit boards designed for the 796 Bus interface should adhere to the following standards (see Fig. 31).

a. The connectors on the bus side of the board will be called P1, P2. P1 is the 86 pin main connector, and P2 is the 60 pin auxiliary connector.

b. Mating connectors on the motherboard (796 Bus) backplane will be called J1, J2, etc.

c. Pins should be numbered with odd number pins on the component side of the board, and in ascending order when going counterclockwise around the board (as shown in Fig. 32).

4.2.2 *Standard Outline of Printed Wiring Boards.* Figure 33 shows the standard outline for 796 Bus-compatible boards (Printed Wire Boards and Printed Circuit Boards). The non-bus edge of the board is not restricted. The remainder of the board including conenctors P1 and P2 must adhere to the dimensions shown in Fig. 33. Only the basic boards' standard vertical height is currently specified.

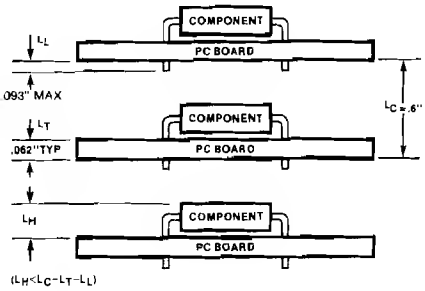
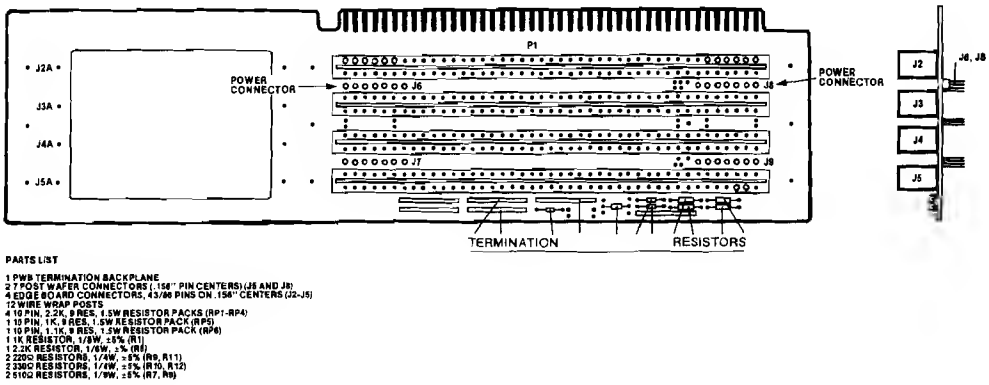


Fig. 30
796 Bus Backplane Card to Card Separation



PARTS LIST

1 PWB TERMINATION BACKPLANE
2 7 POST WAFER CONNECTORS (.156" PIN CENTERS) (J6 AND J8)
4 EDGE BOARD CONNECTORS, 43/86 PINS ON .156" CENTERS (J2-J5)
12 WIRE WRAP POSTS
4 10 PIN, 2.2K, 9 RES, 1.5W RESISTOR PACKS (RP1-RP4)
1 10 PIN, 1K, 9 RES, 1.5W RESISTOR PACK (RP5)
1 10 PIN, 1.1K, 9 RES, 1.5W RESISTOR PACK (RP6)
1 1K RESISTOR, 1/8W, ±5% (R1)
1 2.2K RESISTOR, 1/8W, ±5% (R8)
2 220Ω RESISTORS, 1/4W, ±5% (R9, R11)
2 330Ω RESISTORS, 1/4W, ±5% (R10, R12)
2 510Ω RESISTORS, 1/8W, ±5% (R7, R9)

Fig. 31
Typical 796 Bus Backplane

4.2.3 *Bus Connectors.* The 796 Bus backplane has connectors that mate to the P1 (43/86 pin) board edge connector. The backplane uses 43/86 pin on 0.156" centers connectors.

The P2 connector is a 30/60 pin board edge connector with 0.100" pin centers.

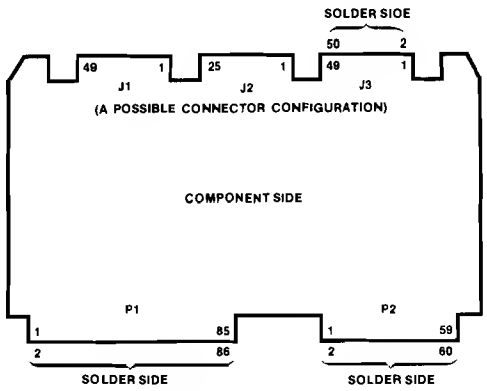


Fig. 32
Connector and Pin Numbering

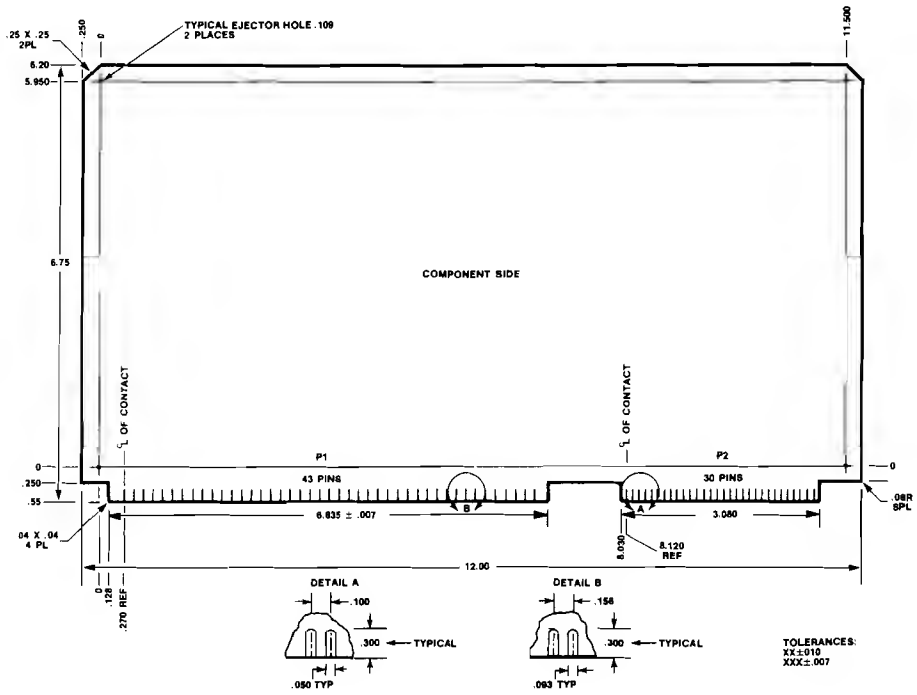


Fig. 33
Standard Printed Wiring Board Outline

Table 4
Pin Assignment of Bus Signals on 796 Bus Board Connector (P1)

	Pin	(Component Side)		Pin	(Circuit Side)	
		Mnemonic	Description		Mnemonic	Description
Power Supplies	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9		Reserved, bussed	10		Reserved, bussed
	11	GND	Signal GND	12	GND	Signal GND
Bus Controls	13	BCLK*	Bus Clock	14	INIT*	Initialize
	15	BPRN*	Bus Pri. In	16	BPRO*	Bus Pri. Out
	17	BUSY*	Bus Busy	18	BREQ*	Bus Request
	19	MRDC*	Mem Read Cmd	20	MWTC*	Mem Write Cmd
	21	IORC*	I/O Read Cmd	22	IOWC*	I/O Write Cmd
	23	XACK*	XFER Acknowledge	24	INH1*	Inhibit 1 (disable RAM)
Bus Controls and Address	25	LOCK*	Lock	26	INH2*	Inhibit 2 (disable PROM or ROM)
	27	BHEN*	Byte High Enable	28	AD10*	
	29	CBRQ*	Common Bus Request	30	AD11*	Address
	31	CCLK*	Constant Clk	32	AD12*	Bus
	33	INTA*	Intr Acknowledge	34	AD13*	
Interrupts	35	INT6*	Parallel	36	INT7*	Parallel
	37	INT4*	Interrupt	38	INT5*	Interrupt
	39	INT2*	Requests	40	INT3*	Requests
	41	INT0*		42	INT1*	
Address	43	ADRE*		44	ADRF*	
	45	ADRC*		46	ADRD*	
	47	ADRA*	Address	48	ADRB*	Address
	49	ADR8*	Bus	50	ADR9*	Bus
	51	ADR6*		52	ADR7*	
	53	ADR4*		54	ADR5*	
	55	ADR2*		56	ADR3*	
	57	ADR0*		58	ADR1*	
Data	59	DATE*		60	DATF*	
	61	DATC*		62	DATD*	
	63	DATA*	Data	64	DATB*	Data
	65	DAT8*	Bus	66	DAT9*	Bus
	67	DAT6*		68	DAT7*	
	69	DAT4*		70	DAT5*	
	71	DAT2*		72	DAT3*	
	73	DAT0*		74	DAT1*	
Power Supplies	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved, bussed	78		Reserved, bussed
	79	−12V	−12Vdc	80	−12V	−12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

All Reserved pins are reserved for future use and should not be used if upwards compatibility is desired.

5.1.4 *Interrupt Attributes.* The 796 Bus (section 2.3) allows for considerable variety in interrupt attributes. A product may support no interrupts, Non Bus Vectored (NBV) interrupts, two cycle bus vectored interrupts, and three cycle bus vectored interrupts. There are two methods of interrupt sensing: the preferred level-triggered; and for historical compatibility only, edge-level-triggered.

Level-Triggered. The active level of the request line indicates an active request. Requiring no edge to trigger an interrupt allows several sources to be attached to a single request line. Sources for level triggered sense inputs should provide a programmatic means to clear the interrupt request.

Edge-Level-Triggered. The transition from the inactive to the active level indicates an active request if and only if the active level is maintained at least until it has been recognized by the master. The requirement for a transition precludes multiple sources on a request line. But, Edge-Level triggering removes the requirement that the source have a programmatic means to clear the interrupt request.

NOTE

Edge-Level-Triggering is described only to allow for historical compatibility. New designs shall use level-triggered interrupt sensing.

A master may support either or both of the above interrupt sensing methods. It is necessary to configure the system such that the sources of the interrupt requests correspond to the interrupt sensing method of the master. Note that a source which is compatible with Level-Triggering is also compatible with Edge-Level triggering.

5.2 Masters and Slaves When constructing 796 Bus systems it is not necessary that all modules have identical capabilities. One may for instance have a master with an 8/16 bit data path and a slave with an 8 bit data path. The system is completely functional, though the application must restrict itself to 8 bit access to the slave.

The key concept when constructing a 796 Bus system is that of required capability versus supplied capability. Each product will provide some set of capability. A transaction between two such products will be restricted to use that capability which is the intersection of the sets of capability of the two products. In some cases the intersection may be null implying fundamental incompatibility. It is the responsibility of the system designer to assure the viability of this intersection.

5.3 Compliance Level Notation. A notation is introduced which allows a vendor to succinctly and accurately specify a product's level of compliance with the 796 Bus standard. For boards which may act as either masters or slaves, the compliance levels must be specified for both cases. Increasing levels of compliance subsume lesser levels for data path width, memory address path width and I/O address path width. Interrupt attributes are listed separately as they are independent of one another. The lack of an element (i.e., no I/O address path) specification normally implies no capability for this element.

5.3.1 *Data Path*

D8 represents an 8 bit data path

D16 represents an 8/16 bit data path

5.3.2 Memory Address Path

M16 represents a 16 bit memory address path

M20 represents a 20 bit memory address path

M24 represents a 24 bit memory address path

5.3.3 *I/O Address Path*

I8 represents an 8 bit I/O address path

I16 represents an 8 or 16 bit I/O address path

5.3.4 *Interrupt Attributes*

V0 represents Non Bus Vectored interrupt requests

V2 represents two cycle bus vectored interrupt requests

V3 represents three cycle bus vectored interrupt requests

E represents Edge-Level triggering only

L represents Level triggering

EL represents Level or Edge-Level triggering

The interrupt attributes notation can be concatenated to represent multiple capabilities.

5.3.5 *An Example* A versatile combination I/O and memory slave board which supports an 8/16 bit data path, a 20 bit memory address, an 8 or 16 bit I/O address, NBV interrupt requests, two and three cycle bus vectored interrupt requests would be specified as follows:

796 Bus Compliance: Slave D16 M20 I16 VO23 L

5.3.6 *Compliance Marking.* The compliance levels of a card shall be clearly marked on the printed circuit board as well as in the printed specifications.

Table 2
796 Bus Timing Specifications Summary

Parameter	Description	Minimum	Maximum	Units	Reference
t_{AH}	Address Hold Time	50		ns	3.2.1, 3.2.2, 3.2.4
t_{AIZ}	Address to Inhibit High Delay	0	100	ns	3.2.3
t_{AS}	Address Setup Time (at slave board)	50		ns	3.2.1, 3.2.2, 3.2.4
t_{BCY}	BCLK* Period	100	∞	ns	3.2.5
t_{BPRNO}	BPRN* to BPRO+	0	30	ns	3.2.5
t_{BPRNS}	BPRN* to ↑BCLK* Setup Time	22		ns	3.2.5
t_{BPRO}	↑BCLK* to BPRO*	0	40	ns	3.2.5
t_{BREQH}	↑BLCK* to BREQ* High Delay	0	35	ns	3.2.5
t_{BREQL}	↑BCLK* to BREQ* Low Delay	0	35	ns	3.2.5
t_{BSYO}	CBRQ*●BUSY* to ↑BUSY		12	μs	3.2.5
t_{BUSY}	BUSY* delay from ↑BCLK*	0	70	ns	3.2.5
t_{BUSYS}	BUSY* to ↑BCLK Setup Time	25		ns	3.2.5
t_{BW}	BCLK* Width	$0.35t_{BCY}$	$0.65t_{BCY}$		3.2.5
t_{CBRO}	↑BCLK* to CBRQ*	0	60	ns	3.2.5
t_{CBRQS}	CBRQ* to ↑BCLK* Setup Time	35		ns	3.2.5
t_{CCY}	CCLK* Period	100	110	ns	3.2.6
t_{CMD}	Command Pulse Width	100	t_{TOUT}	ns	3.2.1, 3.2.2
t_{CMPH}	Command Hold Tie	20		ns	3.2.1, 3.2.2
t_{CPM}	Central Priority Module Resolution Delay (parallel priority)	0	$t_{BCY}-t_{BREQ}-2t_{PD}-t_{BPRNS}-t_{SKEW}$		3.2.5
t_{CSEP}	Command Separation	100		ns	3.2.4, 3.2.6
t_{CW}	CCLK* Width	$0.35t_{CCY}$	$0.65t_{CCY}$	ns	3.2.6
t_{DHR}	Read Data Hold Time	0	65	ns	3.2.1, 3.2.4
t_{DHW}	Write Data Hold Time	50		ns	3.2.2
t_{DS}	Write Data Setup Time	50		ns	3.2.2

Table 2
796 Bus Timing Specifications Summary (Cont'd.)

Parameter	Description	Minimum	Maximum	Units	Reference
t_{DXL}	Read Data Setup Time to XACK*	0		ns	3.2.1, 3.2.4
t_{IAD}	XACK* Disable from Inhibit (internal parameter on an inhibited slave; used to determine t_{XACKA} min.)	0	100 (arbitrary)	ns	2.3.2
t_{ID}	Inhibit Delay	0	100 (recommend <100 ns)	ns	3.2.3
t_{INIT}	INIT* Width	5		ms	3.2.6, 3.2.7
t_{INTA}	INTA* Width	250		ns	3.2.4
t_{LCKH}	LOCK* hold time from command active	100		ns	3.2.6
t_{LCKS}	LOCK+ to command setup time	100		ns	3.2.6
t_{LOCK}	LOCK* Width		12	μs	3.2.6
t_{OUT}	Timeout Delay		dc (∞)	ms	—
t_{PD}	Standard Bus Propagation Delay		3	ns	3.1.2, 3.2.5
t_{SKEW}	BCLK* Skew		t_{PD}		3.2.5
t_{XACK}	XACK* Time (for slaves without inhibit function)	0	8	μs	3.2.1, 3.2.2, 3.2.4
t_{XACKA}	XACK* Time of an Inhibited Slave	t_{IAD} +50 ns	1500	ns	3.2.3
t_{XACKB}	XACK* Time of an Inhibiting Slave	1500	8000	ns	3.2.3
t_{XAH}	XACK* Hold Time	0	65	ns	3.2.1, 3.2.2, 3.2.4
Serial Priority	See 3.2.5				

3.2.1 Read Operations *(I/O and* Memory). A read operation transfers data from memory or from I/O to the master that is controlling the bus (see 2.2.).The lines involved and timing specifications for a read operation are shown in Fig. 18. See the special inhibit oepration in 3.2.3.

3.2.2 Write Operations *(I/O* and Memory). A write operation transfers data from the master controlling the bus to memory or I/O (see 2.2.).Timing for a write operation is shown in Fig. 19. See 3.2.3 for inhibit operations.

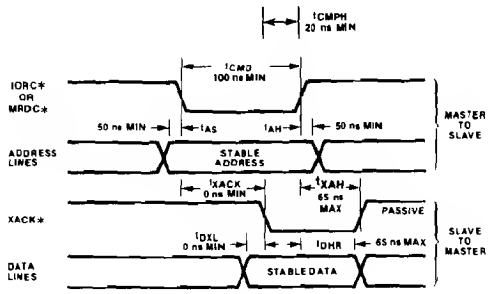


Fig. 18
Read AC Timing

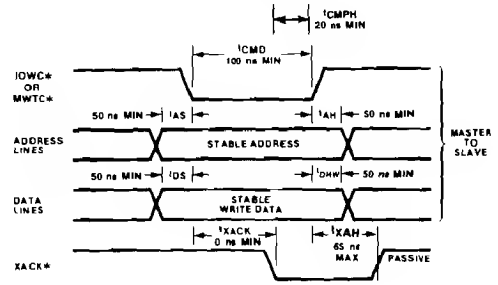


Fig. 19
***Write* AC Timing**

3.2.3 *Inhibit Operations.* An inhibit operation may accompany any memory read or memory write operation. The main effect is for one slave to inhibit another slave from driving the data lines and from returning (driving) an acknowledge (XACK*). I/O addresses cannot be inhibited. Although inhibit signals may be generated during IORC*, IOWC*, or INTA* operations, these signals are ignored by other slaves (including the slave that should respond to the INTA*, IORC-E, or IOWC*). Inhibit timing is as illustrated in Fig. 20. Related subsections are:

Subsection	Number
Functional Descriptions	2.1.3.2.3
Timing Specification Summary	3.2
Read Operations	3.2.1
Write Operations	3.2.2
Interrupt Implementations	3.2.4

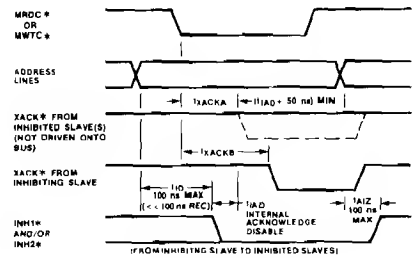


Fig. 20
Inhibit AC Timing

3.2.4 ***Interrupt Implementations.*** There are two types of interrupt implementation schemes: Non-Bus Vectored (NBV) and Bus Vectored (BV).

3.2.4.1 NBV Interrupts. NBV interrupts are handled on the bus master and do not require the 796 Bus for transfer of an interrupt vector address. The slave modules generating the interrupts may reside on the master module or on other bus modules, in which case they use the 796 Bus interrupt request lines (INTO* -INT7*) to generate interrupt requests to the bus master. When an interrupt request line is activated. the bus master performs its own internal interrupt operations and then processes the interrupt.

3.2.4.2 BV Interrupts. BV interrupts are those interrupts that transfer the interrupt vector address along the 796 Bus from the slave to the bus master in response to the INTA* command signal. BV interrupt timing is shown in Fig. 21.

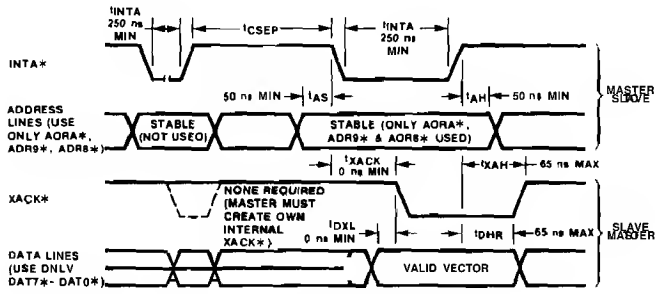


Fig. 21
Bus Vectored (BV) Interrupt AC Timing

When an interrupt request occurs, the interrupt control logic on the bus master interrupts its processor. The processor on the bus master generates an INTA* command, which freezes the state of the interrupt logic on the 796 Bus for priority resolution. The bus master also locks the 796 Bus (retains the bus between bus cycles) to guarantee itself back-to-back bus cycles. After the first INTA* command, the bus master's interrupt control logic puts an interrupt code onto the 796 Bus address lines. The interrupt code is the address of the highest priority active interrupt request line. At this point in the BV interrupt procedure, two different sequences could take place. The difference occurs because the 796 Bus can support masters that generate either two or three INTA* commands during the interrupt process.

If the bus master generates two INTA* commands, one more INTA* command will be generated. This second INTA* causes the bus slave interrupt control logic to transmit its interrupt vector address on the 796 Bus data lines. The address is used by the bus master to service the interrupt.

If the bus master generates three INTA* commands, two more INTA* commands will be generated. These two INTA* commands allow the bus slave to put its 2-byte interrupt vector address onto the data lines (one byte for each INTA* command). The interrupt vector address is used by the bus master to service the interrupt.

NOTE

The 796 Bus can support only one type of BV interrupt in a given system. However, it can support both BV and NBV interrupts in the same system.

Subsections related to BV and NBV interrupts are:

Subsection	Number
Functional Descriptions	2.3.2.2
Timing Specification Summary	3.2

3.2.5 Bus Control Exchanges. A bus control exchange takes control of the bus (i.e., the ability to do read, write, and interrupt acknowledge operations) from one master and gives it to another master. See 2.4 for a functional description of this process.

For a master that does not use the bus signal CBRQ* (Common Bus Request), the timing specifications in Fig. 22 apply.

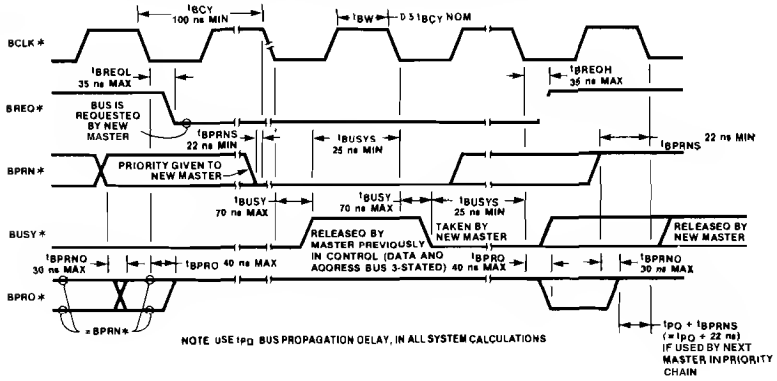


Fig. 22
Bus Exchange AC Timing

For a system using CBRQ* (Common Bus Request), each master must also satisfy the timing requirements illustrated in Fig. **23.** Note that before "releasing the bus" (i.e., releasing BUSY*), the hold times, etc., of any ending cycle must still be met as described in the previous subsections of this chapter. Likewise, after "taking the bus" (i.e., driving BUSY* low), it is necessary to satisfy all applicable setup and other timing parameters for a cycle just beginning.

3.2.5.1 Serial Prrority. For a system that uses a serial priority scheme (i.e., daisy chain BPRO*s to BPRN*s) (see 2.4), the timing specifications in Fig. **24** apply.

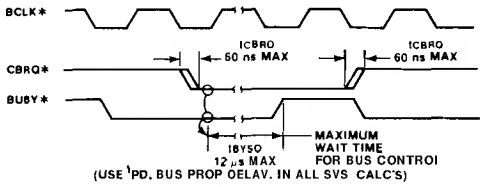


Fig. 23
Common Bus Request AC Timing

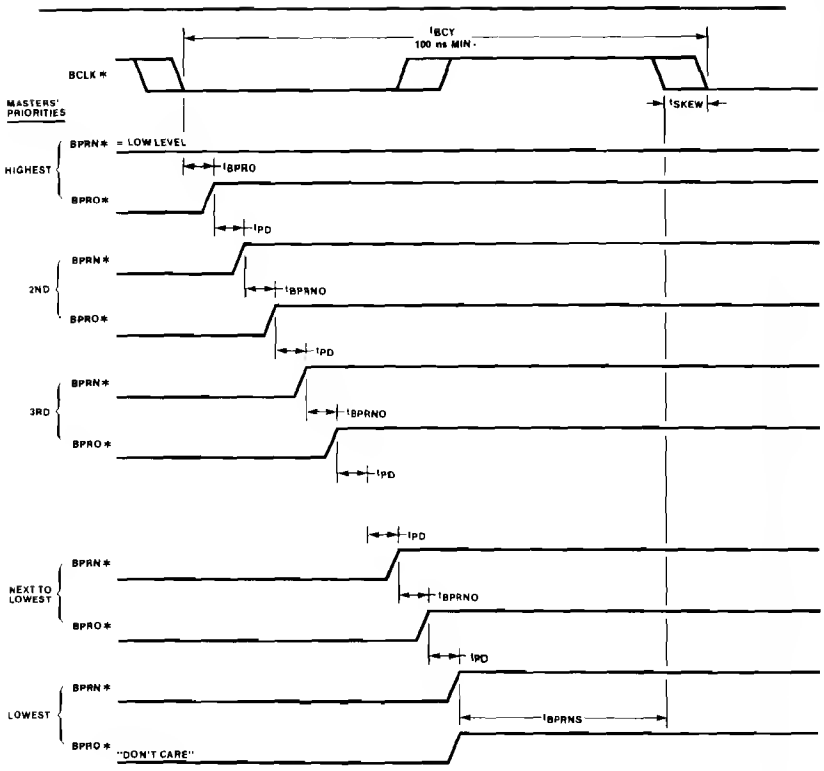


Fig. 24
Serial Priority AC Timing

3.2.5.2 *Parallel Priority.* For a system that uses a parallel priority scheme (i.e., a central priority resolver) (see 2.4), the following system and CPM (Central Priority Module) timing specifications of Fig. 25 apply.

3.2.6 *Miscellaneous Timing.* The timing diagrams in Figs. 26, 27, 28, and 29 show the timing of Constant Clock (CCLK*), Command Separation (t_{CSEP}), Initialize (t_{INIT}), and Lock (LOCK*), respectively.

3.3 Receivers, Drivers and Terminations. Non-timing specifications unique to each signal line or to groups of signal lines are presented in Table 3. The requirementsfor the signal line receivers, drivers, and bus terminations, and the locations of the receiver. driver, and termination for each signal are given.

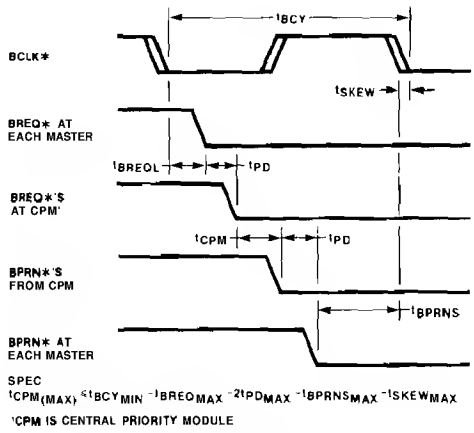


Fig. 25
Parallel Priority AC Timing

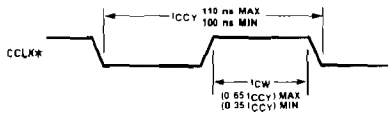


Fig. 26
Constant Clock AC Timing

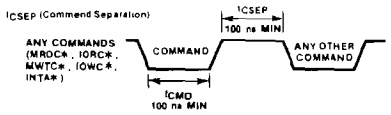


Fig. 27
Command Separation AC Timing

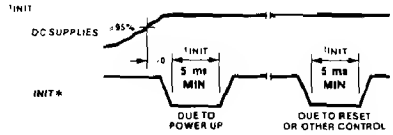


Fig. 28
Initialize AC Timing

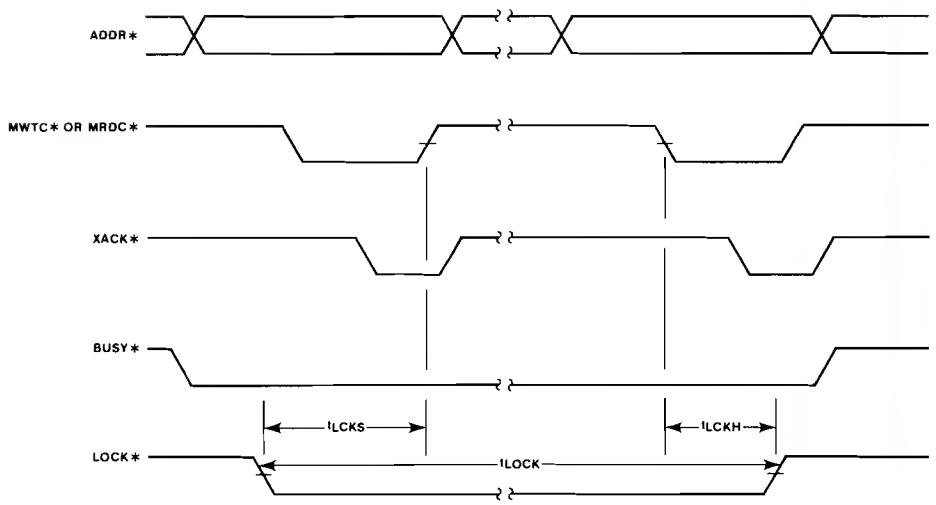


Fig. 29
Lock AC Timing

Table 3
Bus Drivers, Receivers, and Terminations

			Driver[1,3]					Receiver[2,3]				Termination		
Bus Signals	Location	Type	I_{OL} Min_{mA}	I_{OH} $Min_{\mu a}$	I_{OH} $Max_{\mu a}$	C_O Min_{pf}	Location	I_{IL} Max_{mA}	I_{IH} $Max_{\mu a}$	C_I Max_{pf}	Location	Type	R	Units
DAT0* - DATF* (16 lines)	Masters & Slaves	TRI	16	-2000	—	300	Masters & Slaves	-0.8	125	18	1 place	Pullup	2.2	KΩ
ADR0* - ADR17*, BHEN* (25 lines)	Masters	TRI	16	-2000	—	300	Slaves	-0.8	125	18	1 place	Pullup	2.2	KΩ
MRDC*, MWTC*	Masters	TRI	32	-2000	—	300	Slaves (Memory; Memory-Mapped I/O)	-2	125	18	1 place	Pullup	1	KΩ
IORC*, IOWC*	Masters	TRI	32	-2000	—	300	Slaves (I/O)	-2	125	18	1 place	Pullup	1	KΩ
XACK*	Slaves	TRI	32	-400	—	300	Masters	-2	125	18	1 place	Pullup	510	Ω
INH1*, INH2*	Inhibiting Slaves	OC	16	—	-250	300	Inhibited Slaves (RAM, PROM, ROM, Memory-Mapped I/O)	-2	50	18	1 place	Pullup	1	KΩ
BCLK*	1 place (Master usually)	TTL	48	-3000	—	300	Masters	-2	125	18	Motherboard	To +5V To GND	220 330	Ω Ω
BREQ*	Each Master	TTL	10	-200	—	60	Central Priority Module	-2	50	18	Central Priority Module (not req)	Pullup	1	KΩ
BPRO*	Each Master	TTL	3.2	-200	—	60	Next Master in Serial Priority Chain at its BPRN*	-1.6	50	18	(not req)			
BPRN*	Parallel: Central Priority Module Serial: Prev Masters BPRO*	TTL	16	-400	—	300	Masters	-4	100	18	(not req)			

Table 3
Bus Drivers, Receivers, and Terminations (Cont'd.)

		Driver[1,3]					Receiver[2,3]			Termination			
Bus Signals	Location	Type	I_{OL} Min_{mA}	I_{OH} $Min_{\mu a}$	I_{OH} $Max_{\mu a}$	C_O Min_{pf}	Location	I_{IL} Max_{mA}	I_{IH} $Max_{\mu a}$	C_I Max_{pf}	Location[5]	Type	R	Unit
LOCK*	Master	TRI	32	-2000	—	300	All	-2	125	18	1 place	Pullup	1	KΩ
BUSY*, CBRQ*	All Masters	OC	20	—	-250	300	All Masters	-2	50	18	1 place	Pullup	1	KΩ
INIT*	Master	OC	32	—	-250	300	All	-2	50	18	1 place	Pullup	2.2	KΩ
CCLK*	1 place	TTL	48	-3000	—	300	Any	-2	125	18	Mother-board	To +5V	220	Ω
												To GND	330	Ω
INTA*	Masters	TRI	32	-2000	—	300	Slaves (Interrupting I/O)	-2	125	18	1 place	Pullup	1	KΩ
INT0* - INT7* (8 lines)	Slaves	OC	16	—	-250	300	Masters	-1.6	40	18	1 place	Pullup	1	KΩ

[1]Driver Requirements:
- I_{OH} = High Output Current Drive
- I_{OL} = Low Output Current Drive
- C_O = Capacitance Drive Capability
- TRI = 3-State Drive
- OC = Open Collector Driver
- TTL = Totem-pole Driver

[2]Receiver Requirements:
- I_{IH} = High Input Current Load
- I_{IL} = Low Input Current Load
- C_I = Capacitive Load

[3]For low and high voltage specifications see 3.1.1.

[4]±5%, ¼W Resistors

[5]All termination resistors specified as "1 place" are typically located on the motherboard.

This section describes all the physical and mechanical specifications that a designer must be concerned with when designing a 796 Bus backplane or when designing printed circuit boards that will plug into the 796 Bus interface.

4.1 Backplane Considerations. This section is a discussion of the things that the designer must consider when designing a 796 Bus backplane.

The maximum length of the backplane connecting modules is 18 inches. Extender boards used within the system will not be supported by the bus unless the overall resulting length of the bus including the extender card is less than the 18-inch maximum.

4.1.1 Board to Board Relationships. The following printed circuit board specifications must be adhered to when designing 796 Bus compatible boards which are to operate in a 0.6-inch board to board spacing backplane.

a. Board to Board Spacing (L_C) – center to center of boards when plugged into backplane must be at least 0.6 inches ±0.02.

b. Board Thickness (L_T) – the typical board thickness is 0.062 ±0.005 inches.

c. Component Lead Length (L_L) – the length of the component leads below the printed circuit board cannot exceed 0.093 inches.

d. Component Height (L_H) – the following equation is used to determine the maximum height of the components above the printed circuit board:

$L_H < L_C - L_T - L_L$

$L_H < 0.58" - 0.067" - 0.093"$

$L_H < 0.420$ inches (including board warpage)

Electrically conductive components require L_H to be decreased to 0.40 inches.

An example of a typical backplane and the components necessary to implement it are shown in Fig. 31.

This section contains only the mechanical specifications for designing a 796 Bus interface. The designer must also take into consideration the electrical specifications in Section 3.

4.1.2 796 Bus Pin Assignments. Printed circuit boards which are designed to interface to the 796 Bus have two connectors which plug into the backplane. P1 (Primary) and P2 (Auxiliary). Table 4 shows the pin/signal assignments for the P1 connector on the printed circuit boards. Reserved signals on the P1 connector must be bussed as normal signal lines on the backplane. Table 5 shows the pin/signal assignments for the P2 connector on the printed circuit boards. If a backplane is used then the "Reserved and bussed" signals must be bussed as normal signal lines, and the "Reserved but not bussed" signals shall have no connections.

4.2 796 Bus Board Form Factors. Certain 796 Bus characteristics must be taken into consideration when designing printed circuit boards that interface to it. The designer will ensure himself of 796 Bus compatibility if the specifications discussed in this chapter are followed.

4.2.1 Connector Naming and Pin Numbering Standards. The connectors on the printed circuit boards designed for the 796 Bus interface should adhere to the following standards (see Fig. 31).

a. The connectors on the bus side of the board will be called P1, P2. P1 is the 86 pin main connector, and P2 is the 60 pin auxiliary connector.

b. Mating connectors on the motherboard (796 Bus) backplane will be called J1, J2, etc.

c. Pins should be numbered with odd number pins on the component side of the board, and in ascending order when going counterclockwise around the board (as shown in Fig. 32).

4.2.2 Standard Outline of Printed Wiring Boards. Figure 33 shows the standard outline for 796 Bus-compatible boards (Printed Wire Boards and Printed Circuit Boards). The non-bus edge of the board is not restricted. The remainder of the board including conenctors P1 and P2 must adhere to the dimensions shown in Fig. 33. Only the basic boards' standard vertical height is currently specified.

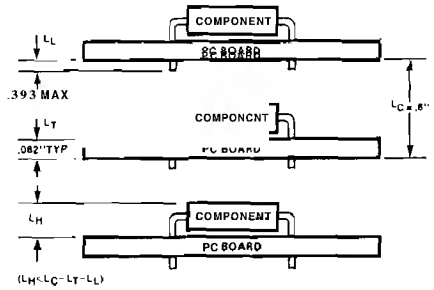
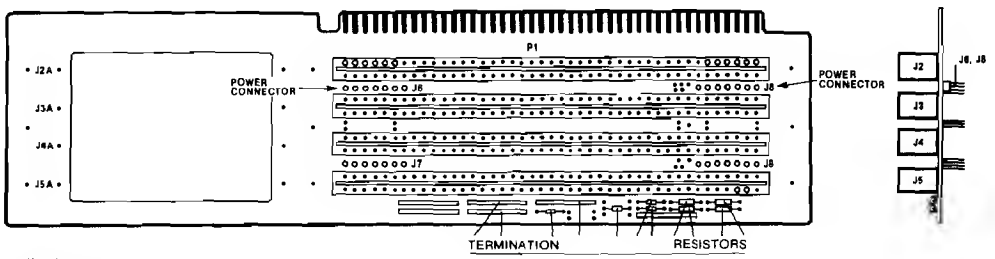


Fig. 30
796 Bus Backplane Card to Card Separation



PARTS LIST

1 PWB TERMINATION BACKPLANE
2 7 POST WAFER CONNECTORS (.156" PIN CENTERS) (J6 AND J8)
4 EDGE BOARD CONNECTORS, 43/86 PINS ON .156" CENTERS (J2-J5)
12 WIRE WRAP POSTS
4 10 PIN, 2.2K, 8 RES, 1.5W RESISTOR PACKS (RP1-RP4)
1 10 PIN, 1K, 9 RES, 1.5W RESISTOR PACK (RP5)
1 10 PIN, 1.1K, 8 RES, 1.5W RESISTOR PACK (RP6)
1 1K RESISTOR, 1/8W, ±5% (R1)
1 2.2K RESISTOR, 1/8W, ±5% (R5)
2 220Ω RESISTORS, 1/4W, ±5% (R8, R11)
2 330Ω RESISTORS, 1/4W, ±5% (R10, R12)
2 510Ω RESISTORS, 1/8W, ±5% (R7, R4)

Fig. 31
Typical 796 Bus Backplane

4.2.3 Bus Connectors. The 796 Bus backplane has connectors that mate to the P1 (43/86 pin) board edge connector. The backplane uses 43186 pin on 0.156" centers connectors.

The P2 connector is a 30/60 pin board edge connector with 0.100" pin centers.

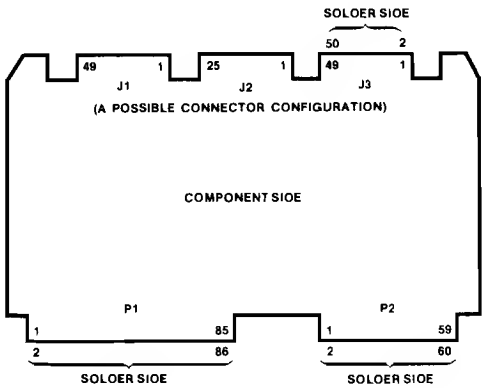


Fig. 32
Connector and Pin Numbering

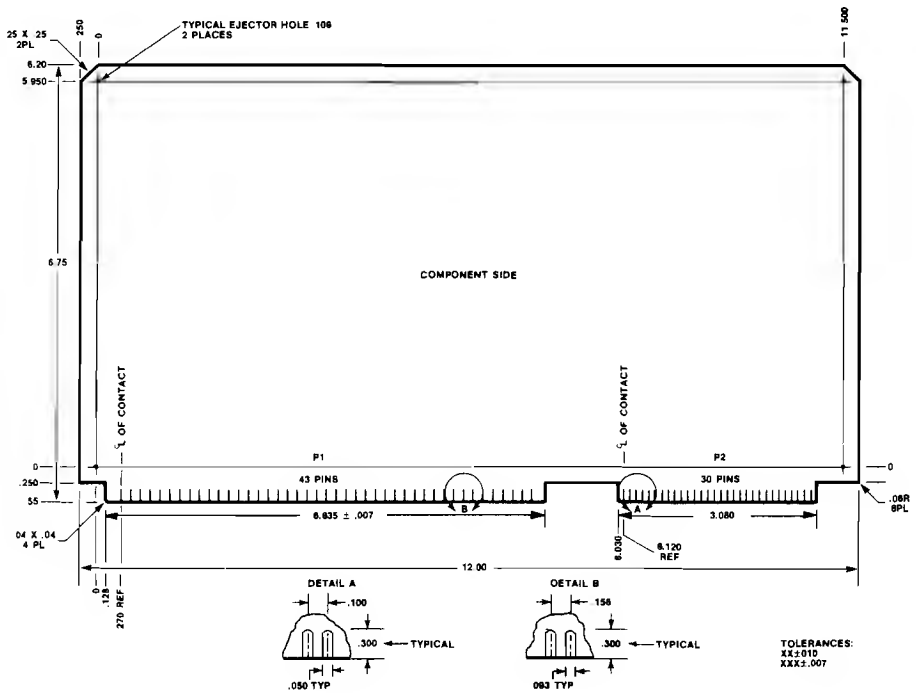


Fig. 33
Standard Printed Wiring Board Outline

Table 4
Pin Assignment of Bus Signals on 796 Bus Board Connector (P1)

	Pin	(Component Side)		Pin	(Circuit Side)	
		Mnemonic	Description		Mnemonic	Description
Power Supplies	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9		Reserved, bussed	10		Reserved, bussed
	11	GND	Signal GND	12	GND	Signal GND
Bus Controls	13	BCLK*	Bus Clock	14	INIT*	Initialize
	15	BPRN*	Bus Pri. In	16	BPRO*	Bus Pri. Out
	17	BUSY*	Bus Busy	18	BREQ*	Bus Request
	19	MRDC*	Mem Read Cmd	20	MWTC*	Mem Write Cmd
	21	IORC*	I/O Read Cmd	22	IOWC*	I/O Write Cmd
	23	XACK*	XFER Acknowledge	24	INH1*	Inhibit 1 (disable RAM)
Bus Controls and Address	25	LOCK*	Lock	26	INH2*	Inhibit 2 (disable PROM or ROM)
	27	BHEN*	Byte High Enable	28	AD10*	
	29	CBRQ*	Common Bus Request	30	AD11*	Address
	31	CCLK*	Constant Clk	32	AD12*	Bus
	33	INTA*	Intr Acknowledge	34	AD13*	
Interrupts	35	INT6*	Parallel	36	INT7*	Parallel
	37	INT4*	Interrupt	38	INT5*	Interrupt
	39	INT2*	Requests	40	INT3*	Requests
	41	INT0*		42	INT1*	
Address	43	ADRE*		44	ADRF*	
	45	ADRC*		46	ADRD*	
	47	ADRA*	Address	48	ADRB*	Address
	49	ADR8*	Bus	50	ADR9*	Bus
	51	ADR6*		52	ADR7*	
	53	ADR4*		54	ADR5*	
	55	ADR2*		56	ADR3*	
	57	ADR0*		58	ADR1*	
Data	59	DATE*		60	DATF*	
	61	DATC*		62	DATD*	
	63	DATA*	Data	64	DATB*	Data
	65	DAT8*	Bus	66	DAT9*	Bus
	67	DAT6*		68	DAT7*	
	69	DAT4*		70	DAT5*	
	71	DAT2*		72	DAT3*	
	73	DAT0*		74	DAT1*	
Power Supplies	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved, bussed	78		Reserved, bussed
	79	−12V	−12Vdc	80	−12V	−12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

All Reserved pins are reserved for future use and should not be used if upwards compatibility is desired.

5.1.4 Interrupt Attributes. The *796* Bus (section **2.3**)allows for considerable variety in interrupt attributes. A product may support no interrupts, Non Bus Vectored (NBV) interrupts, two cycle bus vectored interrupts, and three cycle bus vectored interrupts. There are two methods of interrupt sensing: the preferred level-triggered; and for historical compatibility only, edge-level-triggered.

Level-Triggered. The active level of the request line indicates an active request. Requiring no edge to trigger an interrupt allows several sources to be attached to a single request line. Sources for level triggered sense inputs should provide a programmatic means to clear the interrupt request.

Edge-Level-Triggered. The transition from the inactive to the active level indicates an active request if and only if the active level is maintained at least until it has been recognized by the master. The requirement for a transition precludes multiple sources on a request line. But, Edge-Level triggering removes the requirement that the source have a programmatic means to clear the interrupt request.

NOTE

Edge-Level-Triggering is described only to allow for historical compatibility New designs shall use level-triggered interrupt sensing.

A master may support either or both of the above interrupt sensing methods. It is necessary to configure the system such that the sources of the interrupt requests correspond to the interrupt sensing method of the master. Note that a source which is compatible with Level-Triggering is also compatible with Edge-Level triggering.

5.2 Masters **and** Slaves When constructing 796 Bus systems it is not necessary that all modules have identical capabilities. One may for instance have a master with an 8/16 bit data path and a slave with an 8 bit data path. The system is completely functional, though the application must restrict itself to 8 bit access to the slave.

The key concept when constructing a 796 Bus system is that of required capability versus supplied capability. Each product will provide some set of capability. A transaction between two such products will be restricted to use that capability which is the intersection of the sets of capability of the two products. In some cases the intersection may be null implying fundamental incompatibility. It is the responsibility of the system designer to assure the viability of this intersection.

5.3 Compliance Level Notation. A notation is introduced which allows a vendor to succinctly and accurately specify a product's level of compliance with the 796 Bus standard. For boards which may act as either masters or slaves, the compliance levels must be specified for both cases. Increasing levels of compliance subsume lesser levels for data path width, memory address path width and I/O address path width. Interrupt attributes are listed separately as they are independent of one another. The lack of an element (i.e., no I/O address path) specification normally implies no capability for this element.

5.3.1 *Data Path*

D8	represents an 8 bit data path
D16	represents an 8/16 bit data path

5.3.2 Memory Address Path

M16	represents a 16 bit memory address path
M20	represents a 20 bit memory address path
M24	represents a 24 bit memory address path

5.3.3 I/O Address Path

I8	represents an 8 bit I/O address path
I16	represents an 8 or 16 bit I/O address path

5.3.4 *Interrupt Attributes*

V0	represents Non Bus Vectored interrupt requests
V2	represents two cycle bus vectored interrupt requests
V3	represents three cycle bus vectored interrupt requests
E	represents Edge-Level triggering only
L	represents Level triggering
EL	represents Level or Edge-Level triggering

The interrupt attributes notation can be concatenated to represent multiple capabilities.

5.3.5 An Example A versatile combination I/O and memory slave board which supports an 8/16 hit data path, a 20 bit memory address, an A or 16 bit I/O address, NBV interrupt requests, two and three cycle bus vectored interrupt requests would be specified as follows:

796 Bus Compliance: Slave D16 M20 116 V023 L

5.3.6 Compliance Marking. The compliance levels of a card shall be clearly marked on the printed circuit board as well as in the printed specifications.